SERIAL DRUMS
250/251

INSTRUCTION MANUAL

VOLUME 1

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PREFACE

This manual, comprising two volumes, contains information on the principles of operation, installation, operation, programming, and maintenance of the Digital Equipment Corporation Serial Drums Type 250 and Type 251. The serial drum is designed for use as a data storage device to augment the main memory of a computing system. Chapter 1 (Volume 1) presents information of a general nature which is applicable to the entire machine. Chapter 2 explains the principles of operation of the serial drum as a system and each functional element of the system. Chapters 3 through 6 present information and procedures which allow personnel to install, operate, program, and maintain the equipment. Reference material pertaining to the engineering drawings of the machine is contained in Chapter 7 (Volume 2).

CONTENTS

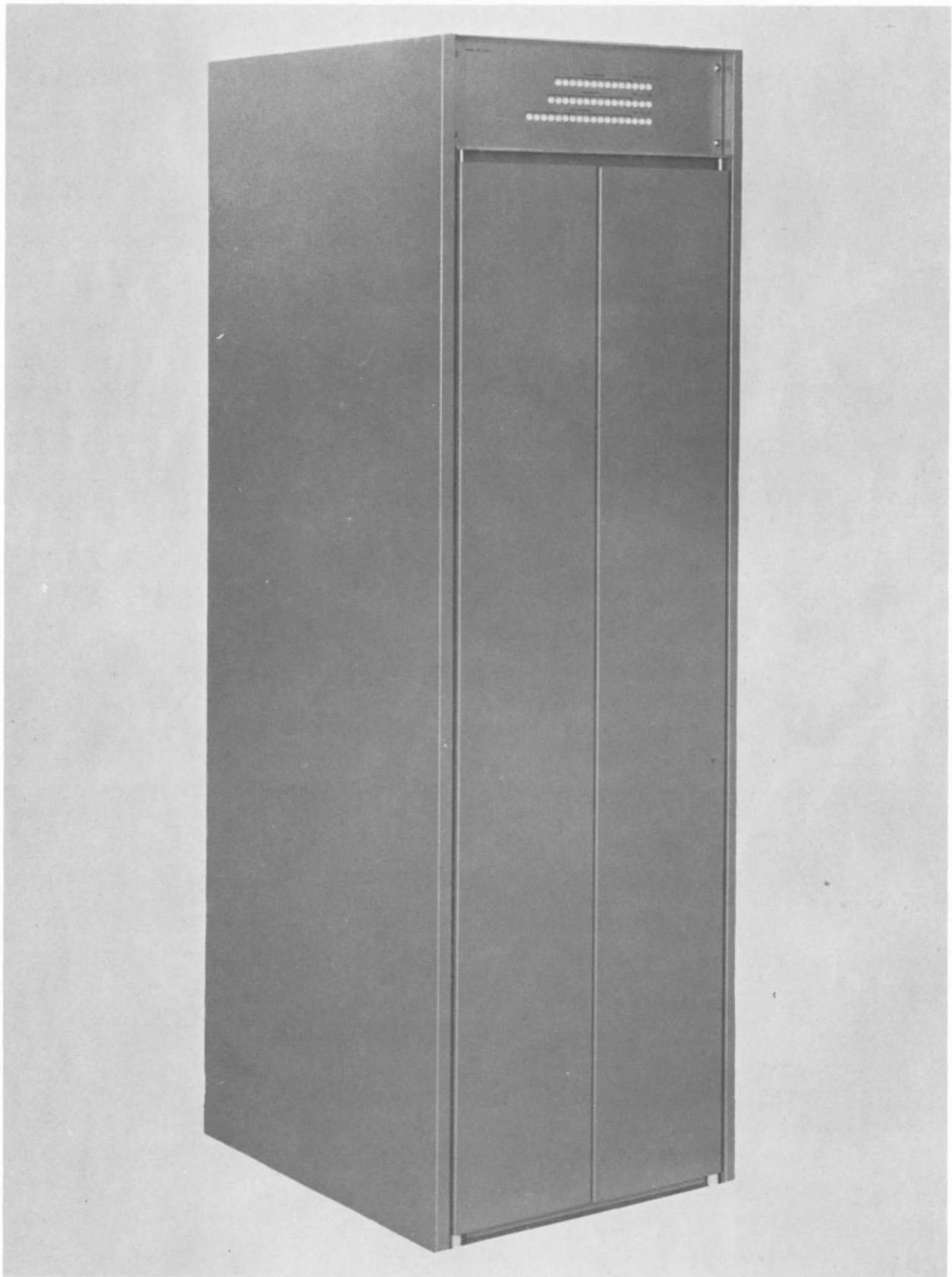
CONTENTS (Continued)

CONTENTS (Continued)

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

TABLES



Serial Drum Type 250

CHAPTER 1
INTRODUCTION

This manual provides the information necessary for understanding and maintaining the Type 250 and 251 Serial Drum Systems. The manual comprises two volumes: Volume I containing instructive and maintenance text, with appropriate illustrations and reference data; and Volume II, containing system engineering drawings.

This manual (Volume I) describes both the Type 250 Serial Drum, which is used with the Programmed Data Processor (PDP ®)-5 computer, and the Type 251 Serial Drum, which is used with the PDP-8 computer. The two drum systems are almost identical; where they differ, the text points out the difference. Volume II contains engineering drawings for both the 250 and the 251 Drum Systems. Drawing numbers show the 250 or 251 designation; drawings without this designation pertain to both systems.

The Digital Equipment Corporation (DEC) serial drum system serves as an auxiliary data storage device for either the PDP-5 or PDP-8 computer. Information from the computer is stored (written) in the serial drum and retrieved (read) in blocks (sectors) of 128 computer words. After programmed initialization, the system automatically transfers 128-word sectors of data between the computer and the serial drum; interleaving the transfer of each word with the running computer program. Drun systems are available with 8, 16, 32, 64, 128, 192 or 256 tracks; each track holds 8 sectors of 128 words. Each word is transferred in parallel (twelve bits at a time) between the computer and the serial drum, and is written or read on the drum surface in series (one bit at a time).

1.1 FUNCTIONAL DESCRIPTION

The basic functions of the serial drum are data storage and retrieval, core memory address control, track selection data request and transfer control, error checking, and power supply and distribution. Input/output transfer (IOT) instructions from the computer initiate functional operation of the machine by producing the IOT pulses required to enact a sector transfer between the computer and the serial drum.

Under program control, the IOT instructions set up the drum control to transfer data. When the instructions specify the write cycle, these set a memory start address into a register in the serial drum. The memory address increments automatically after each word transfer to the serial drum from the computer. The track and sector address is also set in a register in the serial drum. The setup

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instruction initiates a data break cycle to transfer a 12-bit word to the serial drum from the addressed core memory location. A parity bit is generated for each 12-bit word so that a 13-bit word is written on the drum surface. After a 13-bit word has been written, the data break cycle is entered to obtain the next word. Following the writing of 128 words of the addressed sector, a flag is set to signify the completion of the sector transfer. The track and sector address register increments by one to simplify programming of continuous sector transfers.

When the program specifies a read cycle, a similar routine sets up the serial drum. The memory start address is set into the serial drum memory address register, and the track and sector address is set into the appropriate serial drum register. After a word is read from the addressed drum location, the data break cycle is entered to transfer the word to core memory in the computer. When all 128 words of the addressed sector have been transferred, a flag is set to indicate the completion of the sector transfer.

Error circuits in the serial drum check for parity error during read cycles, and check data transmission timing during both read and write cycles. If bits are picked up or dropped out, if data received from the computer is late during a write cycle, or if data is late in being stored in the core memory during a write cycle, an error signal is sent to the computer (via the clock error IOT).

A power supply and distribution network within the serial drum produces and controls the operating voltages required by all circuits of the machine. The external ac power required to energize the machine is supplied by the PDP-5 for the 250 Drum System and by a 115 vac outlet for the 251 Drum System. Local or remote control of the ac source within each drum system is possible.

1.2 PHYSICAL DESCRIPTION

The Serial Drum System Type 250 is contained in a DEC computer cabinet 21-5/8 inches wide, 25-3/4 inches deep, and 67-7/16 inches high. An indicator panel that exhibits the track address, core location, and drum control status is located at the front of the machine. Maintenance controls are located on the plenum door inside the double rear doors. Power and signal cables enter through a port in the bottom of the cabinet. Four casters allow mobility of the machine, which weighs 500 pounds.

The cabinet is constructed of a welded steel frame covered with sheet steel. Double front and rear doors are held closed by magnetic latches. A full-width plenum door provides mounting for the power supply and switch panel inside the double rear doors. The plenum door is latched by a spring-loaded pin at the top. The indicator panel, racks of logic, and cable connector panel are attached to the front of the cabinet. Module racks are mounted on the front of the cabinet with the wiring side outward, so that modules are accessible by opening the plenum door. A fan mounted at the bottom of the cabinet draws cooling air through a dust filter. The memory drum housing is permanently mounted on braces above the fan assembly.

A coordinant system locates racks, modules, cable connectors, and terminals. Each 5-1/4 inch position on the front of the cabinet is assigned a capital letter, beginning with A at the top, as indicated on figures 1-1 and 1-2. Modules are numbered from 1 through 25 from left to right in a rack, as viewed from the wiring side. Connectors are numbered from 1 through 6 from left to right, as viewed from the front of the machine. Blank module and connector locations are numbered. Terminals on a module connector are designated by capital letters from top to bottom. Therefore, D09E is in the fourth location from the top (D), the ninth module from the left (09), and the fifth (E) terminal from the top of the module. Components mounted on the plenum door are not identified by location.

1.3 SPECIFICATIONS

Dimensions	23-1/2 inches wide, 27-1/6 inches deep, 69-1/8 inches high
Service Clearances	8-3/4 inches in front, 14-7/8 inches in back
Weight	500 lbs
Power Required	115v, 60-hz, single phase, 8-amp starting current, 5-amp running current
Power Dissipation	450w
Power Control Point	Local or remote (computer)
Signal Cables	Two, 50 wire, twisted pair
Temperature	32 to 105°F operating range
Drum Motor	115v, single phase, 2 pole, induction capacitor start and run
Write Current	100 ma
Drum Speed	3600 rpm
Word Transfer Time	132 μsec
Sector Transfer Cycle	17.3 msec

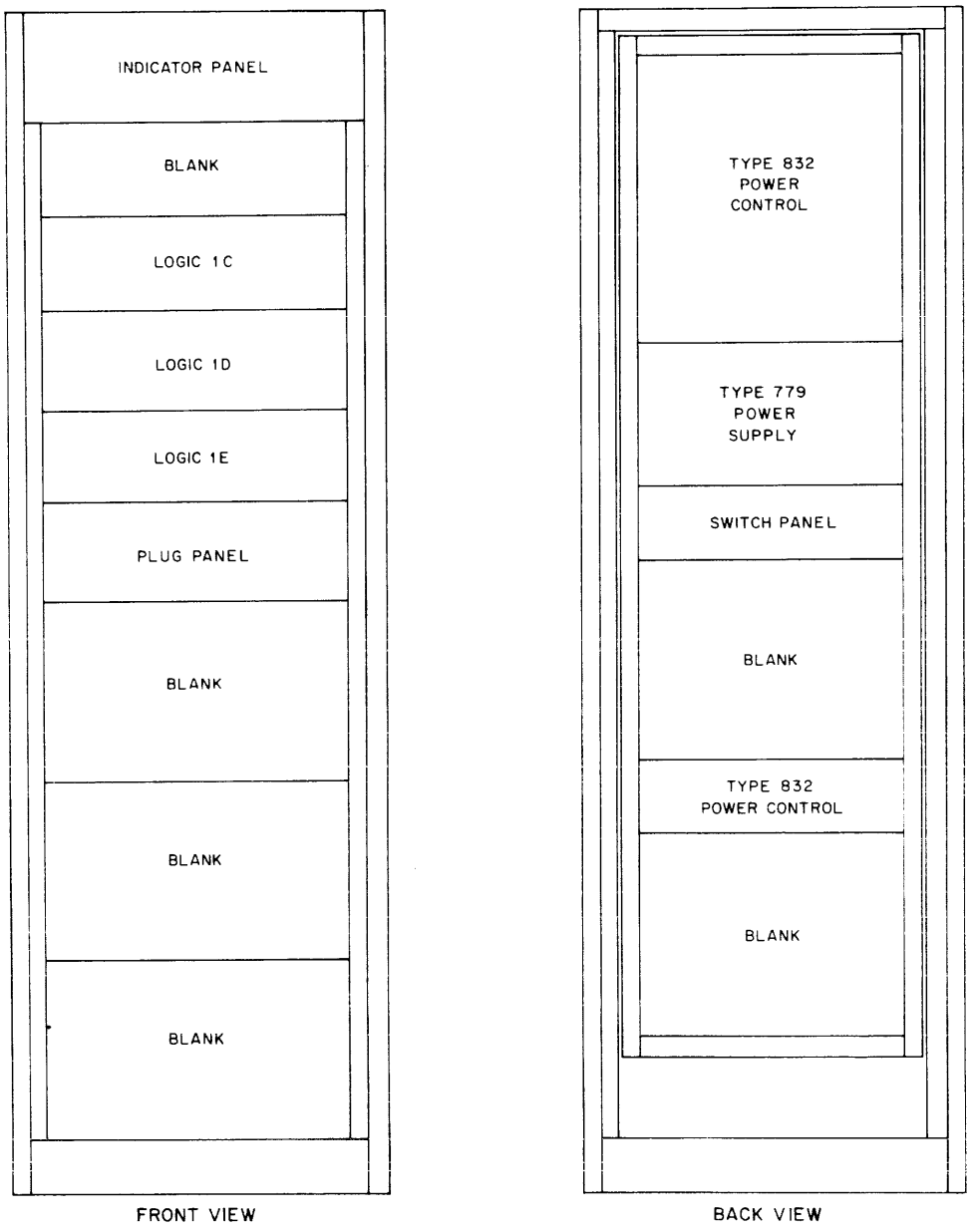

Figure 1-1 Component Locations, 250 Serial Drum

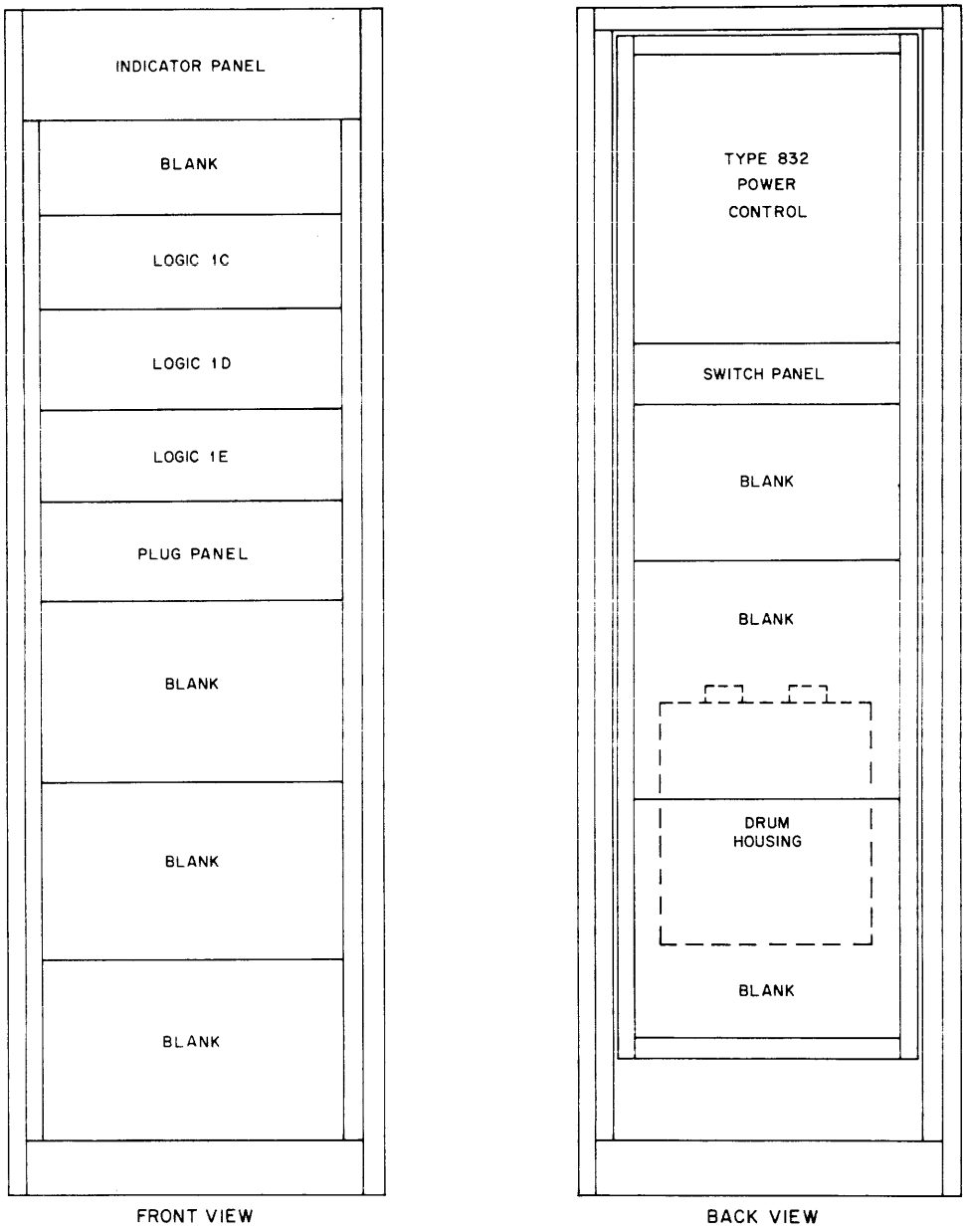

Figure 1-2 Component Locations, 251 Serial Drum

1.4 ABBREVIATIONS

The following abbreviations are used throughout this manual and on engineering drawings.

AC	Accumulator in computer
ACT	Active
AMP	Amplifier
COND	Condition
CLR	Clear
DCL	Drum core location counter in serial drum
DCT	Drum control element in serial drum
DDC	Drum data channel in serial drum
DE	Data error
DF and DFB	Drum final buffer in serial drum
DS	Device selector in serial drum
DSA	Drum sector address
DTA	Drum track address
INT	Interrupt control in computer
IOT	Input/output transfer
MA and MAR	Memory address register in computer
MB	Memory buffer register in computer
PA	Pulse amplifier
PAR	Parity
PE	Parity error
PG	Pulse generator
RQ	Request flip-flop
R PARITY	Read/write parity flip-flop in serial drum
SC	Sector counter in serial drum
SA	Sense amplifier
TRA	Transfer

1.5 REFERENCE DOCUMENTS

The following documents are pertinent to the 250 and 251 Serial Drum Systems.

PDP-5 Handbook, F-55	PDP-5 Maintenance Manual, F-57
PDP-8 Users Handbook, F-85	PDP-8 Maintenance Manual, F-87
System Modules Catalog, C-100	FLIP CHIP™ Modules Catalog, C-105

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CHAPTER 2
PRINCIPLES OF OPERATION

2.1 RECORDING AND PLAYBACK TECHNIQUE

The recording and playback technique employed by the Type 250 and 251 Serial Drums is non-return-to-zero (NRZ) phase modulation. This technique records binary 1s and 0s by controlling the direction of flux change on the drum surface. For example, a flux change in one direction represents a 1; a flux change in the opposite direction represents a 0.

To clarify this point, consider the timing diagram figure 2-1 and the simplified logic diagram figure 2-2. As these drawings show, a positive voltage swing (identified by the arrow) from the write flip-flop produces a flux change to write a 1; a negative voltage swing produces a flux change to write a 0. The read/write circuits are synchronized so that recording occurs on the phase A (0A) time pulse. The write flip-flop must be in a state that permits the phase A pulse to complement the flip-flop to write the specified bit. The phase B (0B) pulse shifts the bit to be written into the last bit of the data register, the DSB0 flip-flop. The delayed phase B pulse senses the DSB0 bit, to put the write flip-flop in the proper state, so that the next phase A pulse complements the write flip-flop to write the bit specified by DSB0.

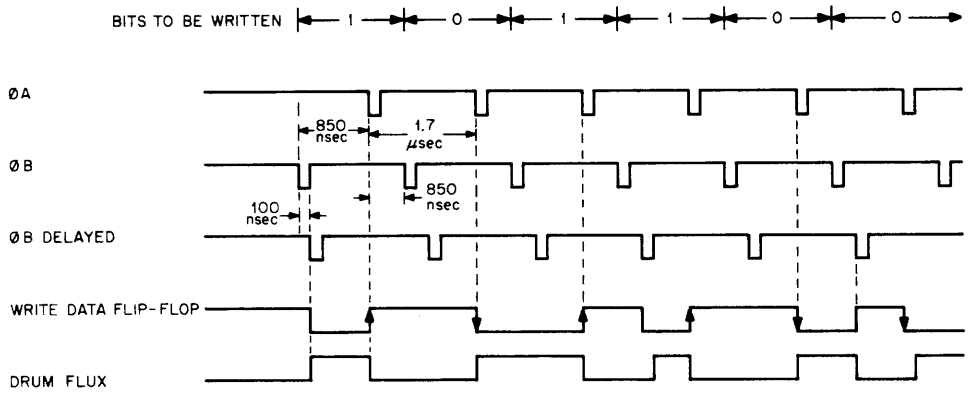


Figure 2-1 Simplified Timing of NRZ Writing

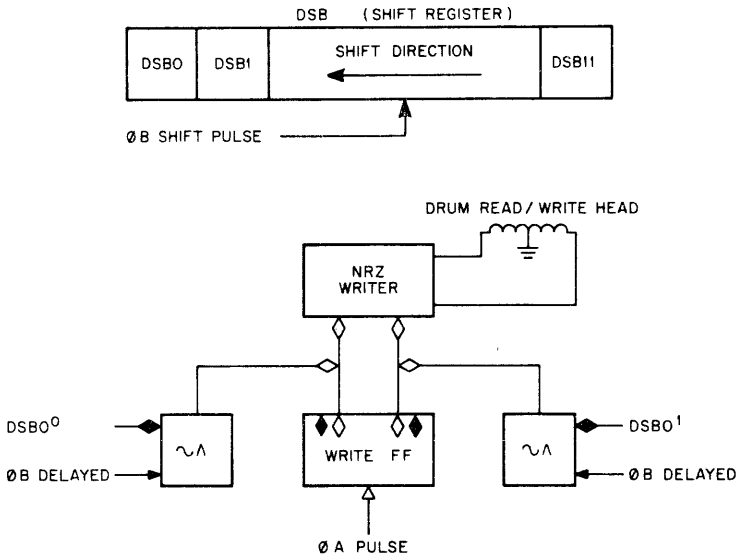


Figure 2-2 Simplified Logic of Writing Circuits

It is clear that when the state of the write flip-flop is switched by the delayed phase B pulse, it causes a flux change on the drum surface. This flux change is not sensed as a binary 1 bit, however, because during playback (reading) the drum is sensed for a flux change only at phase A time. Detailed information on the principle of NRZ recording using phase modulation is shown in figure 2-3.

2.2 DRUM FORMAT

Data from the computer is written on drum tracks that circumscribe the drum cyclinder, as shown in figure 2-4. Both the 250 and 251 Drum Systems are available with 8, 16, 32, 64, 128, 192, or 256 tracks. Each data track contains eight sectors, and each sector contains 128 13-bit words. The 13-bit word consists of 12 data bits, plus a parity bit used only in the drum system.

The words within any particular sector are not stored consecutively on the track. Rather, every eighth word is peculiar to a sector. For example, the first eight words are words 1 for sectors 0 through 7; the next eight words are words 2 for sectors 0 through 7; etc. Consequently, the last eight words on the drum track are words 128 for sectors 0 through 7. Every fourth word is peculiar to a sector in the 251 Drum. Sectors 0 through 3 are on the first half of the track; then a 40-μsec gap separates sectors 4 through 7 on the second half of the track. Each word is transferred in approximately 132 μsec; a sector transfer is completed in approximately 17.3 msec.

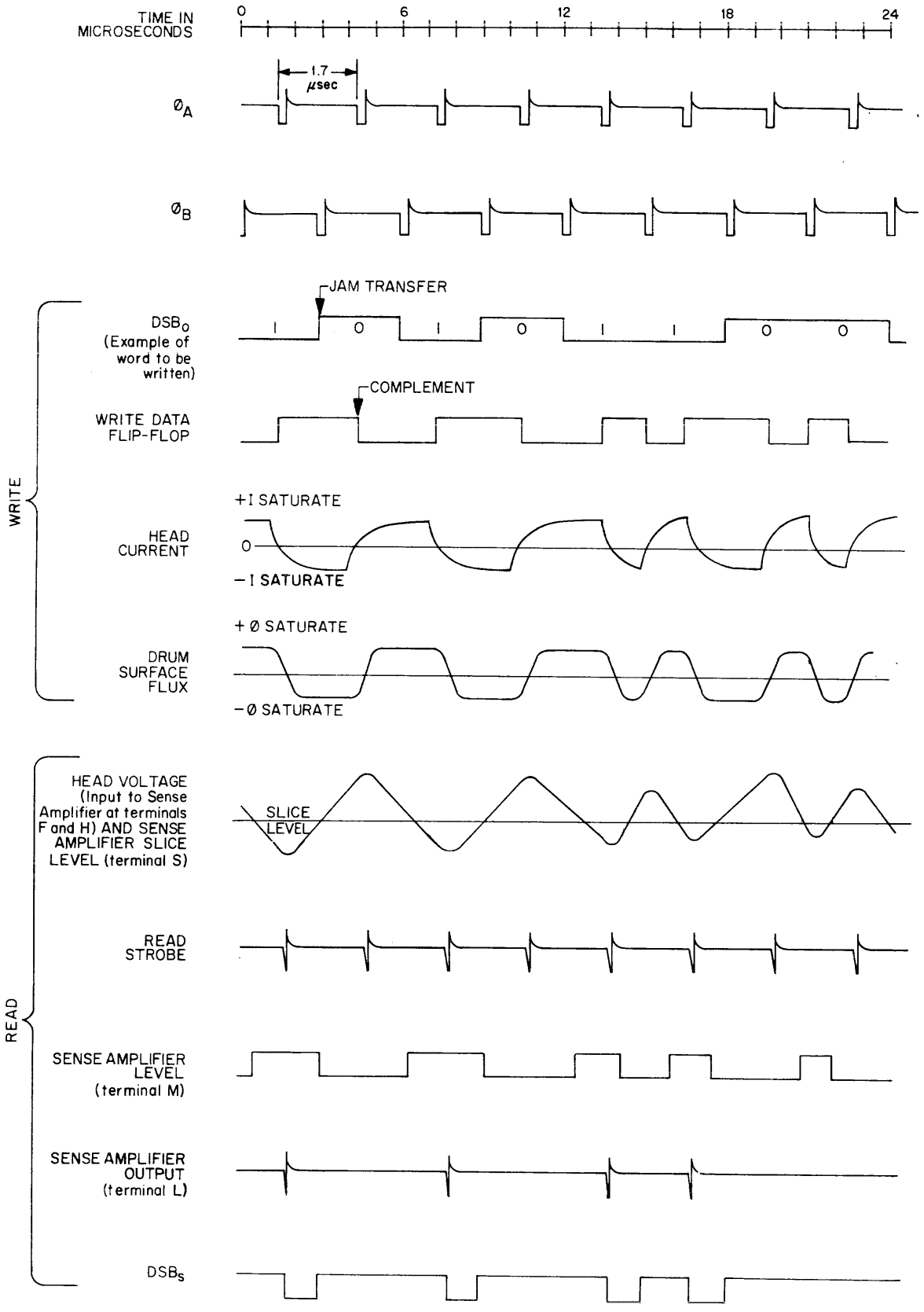
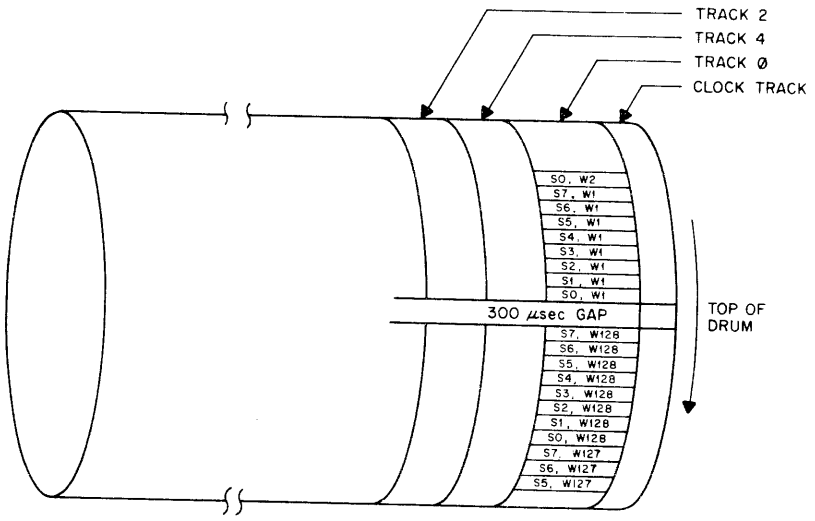


Figure 2-3 Typical Recording and Playback Timing



Drum Track Format

WORDS 3 OF SECTORS 0-7	WORDS 2 OF SECTORS 0-8	WORD 1 OF SECTORS 0-7	GAP	WORDS 128 OF SECTORS 0-7	WORDS 127 OF SECTORS 0-7	WORDS 126 OF SECTORS 0-7

Plane View of Drum Track Format

Figure 2-4 Drum Format

The drum also contains a clock pulse track, which supplies clock pulses to the drum control logic at 1.2-μsec intervals to synchronize writing and reading of the drum. A 300-μsec gap, where no clock pulses exist, separates the beginning and end of each track.

Figure 2-5 shows a closer view of a typical 13-bit word. The word shown is the first word of the track, word 1 of sector 0. The first clock pulse (index pulse) following the 300-μsec gap does not write a bit; it alerts the drum control circuits of the beginning of timing pulses. The next twelve drum clock pulses write the twelve data bits of the word. After twelve bits are written, an odd parity bit is written; i.e., if the twelve bits contain an even number of 1's, a parity bit of 1 is written to generate odd parity. To separate words written on the drum, the 14th drum clock pulse does not write a bit, thus providing a 2.4-μsec gap between words.

There are 14 drum clock pulses per word throughout the entire drum track. This remains true even though the first clock pulse does not record a bit. The last word written does not contain a gap, and consequently no clock pulse is needed; therefore, it requires only 13 clock pulses. This makes up for the index pulse so that there are 14 clock pulses per word throughout the drum track.

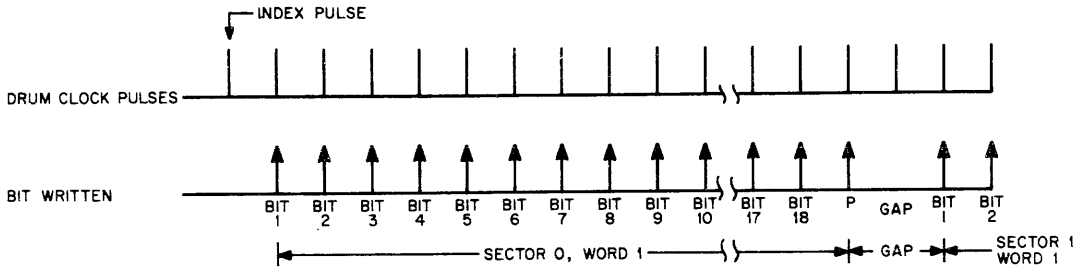


Figure 2-5 Sector Word Format

2.3 BLOCK DIAGRAM DISCUSSION

Major functional elements of the serial drum are shown in figure 2-6. Detailed engineering block schematic diagrams for the serial drum logic are contained in Volume II; references in text are to the engineering drawing numbers. Complete information transfer flow and timing of operations in the 250 Serial Drum are indicated in engineering drawings FD-D-250-0-18 and TD-D-250-0-21, and in the 251 Serial Drum in drawings FD-D-251-0-10 and TD-D-251-0-9 (see chapter 7).

2.3.1 Device Selector (DS)

During the execution of an IOT instruction, the device selector receives MB bits 3 through 8 and the IOP1, IOP2, and IOP4 pulses from the computer. The internal structure of the device selector, which consists of three Type 4605 modules, permits it to generate the IOT pulses controlling the drum circuits during an IOT instruction. The device selector is shown in the lower right corner of engineering drawing BS-D-250-5 for the 250 and drawing BS-D-251-0-4 for the 251.

2.3.2 Drum Core Location Counter (DCL)

The DCL, shown on engineering drawing BS-D-250-0-4 (BS-D-251-0-3)*, is a 15-bit register containing the computer core memory address to or from which the next word is to be transferred. Before transfer of the initial word in a block, the address of the first word is set into the DCL from the computer accumulator under program control. As each word is transferred, the contents of the DCL are automatically incremented by one.

2.3.3 Drum Track and Sector Address Registers (DTA and DSA)

The DTA and DSA registers contain the address of the drum track and sector, respectively, for transfer of a sector. The drum track and sector are set into the serial drum, during program

* The drawing numbers in parentheses refer to the 251 System.

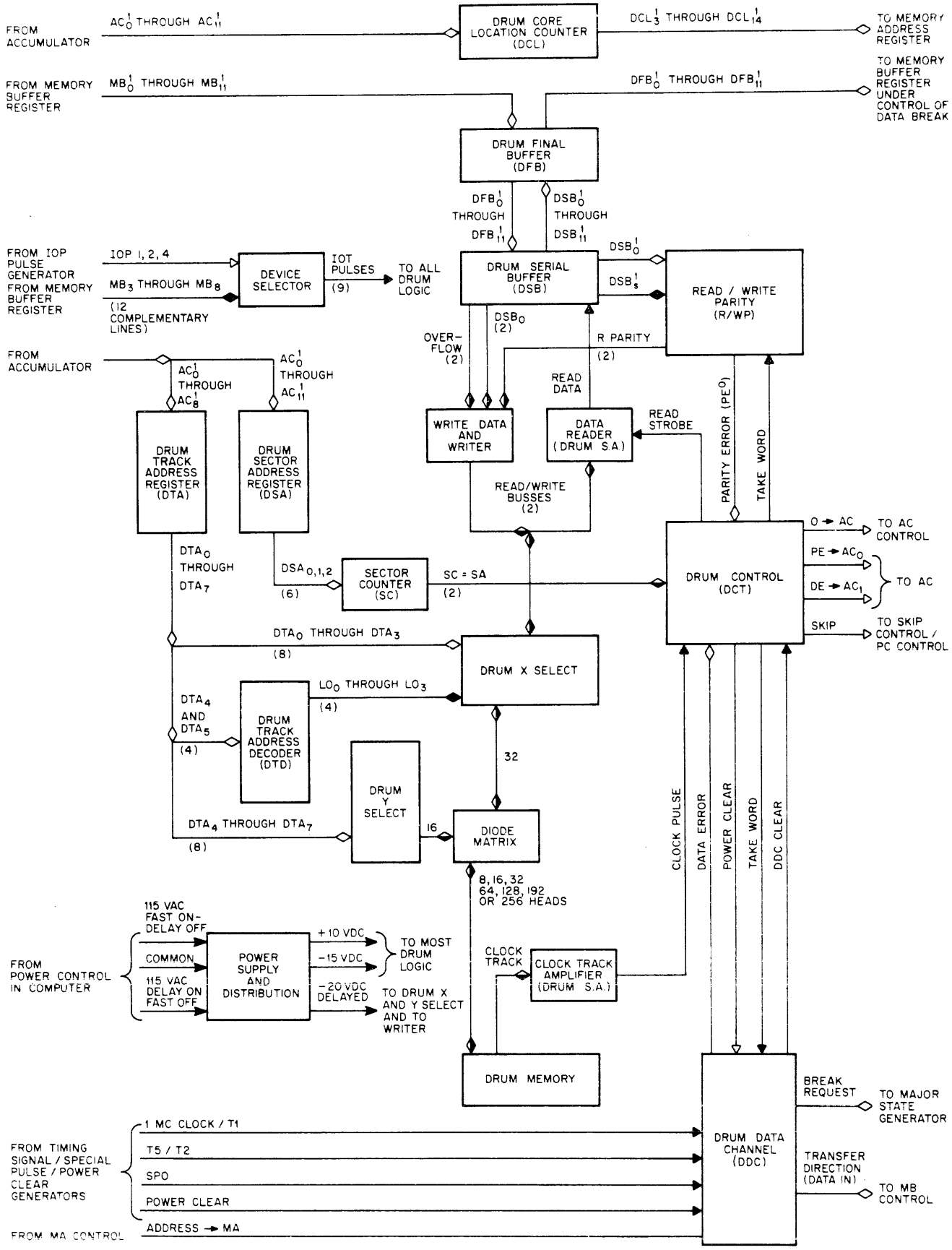


Figure 2-6 Serial Drum Block Diagram

initialization, from the computer accumulator. At the completion of a successful sector transfer, the DTA and DSA contents increment by one to simplify programming of continuous transfer of successive sectors. Engineering drawing BS-D-250-0-4 (BS-D-251-0-3) shows the DTA and DSA detailed logic.

2.3.4 Drum Head Selection

The drum X and Y select circuits, shown on engineering drawing BS-E-250-0-6 (BS-E-251-0-2) and the diode matrix within the drum housing select a drum head. The eight FIELD LOCKOUT switches, when closed, inhibit the X0 and X1 selection modules, to prevent writing on certain tracks which may contain data the programmer wishes to preserve. Each switch inhibits writing on four tracks.

2.3.5 Drum Sense Amplifiers

Two Drum Sense Amplifier Type 1537 Modules convert NRZ signals sensed by the magnetic heads of the drum into digital pulse data. Information recorded on a clock track is sensed by the clock head, and supplied to the sense amplifier, shown on drawing BS-D-250-0-5 (BS-D-251-0-4) as the clock track amplifier. The output from this sense amplifier is applied to the drum control (DCT) to establish the basic clock rate of all drum operations. The sense amplifier, shown on drawing BS-E-250-0-7 (BS-E-251-0-5) as the reader, samples the signals induced on the selected data head. When the read strobe occurs during the maximum negative excursion of the head signal, the SA produces a pulse to set a 1 into the drum serial buffer (DSB).

2.3.6 Drum Control (DCT)

The basic timing pulses for the machine are generated in the DCT from pulses received from the clock track amplifier. The DCT also contains a 4-state device consisting of four negative diode gates. Each state of this device corresponds with and initiates one of the machine control states: idle, transfer (TRA), active (ACT), or transfer done (FLAG). This logic is shown on engineering drawing BS-D-250-0-5 (BS-D-251-0-4).

2.3.7 Drum Data Control (DDC)

Engineering drawing BS-D-250-0-5 (BS-D-251-0-4) shows the DDC. Circuits within the DDC control the transfer of each word between the computer and the drum serial buffer. The DDC establishes the read/write status of the machine, makes the data break request for a computer break cycle, indicates the detection of an error, and designates the direction of the ensuring data transfer.

2.3.8 Drum Final Buffer (DFB)

The DFB is a 12-bit register which serves as a data buffer between the computer memory buffer register and the drum serial buffer. Words are transferred in parallel (twelve bits at a time)

under control of the computer data break control. During drum writing, the DFB holds the next word. During drum reading, the DFB is empty, and is prepared to accept information read from the DSB and place it into the memory buffer under control of the data break control. The DFB logic is shown on engineering drawing BS-E-250-0-7 (BS-E-251-0-5).

2.3.9 Read/Write Parity (R PARITY)

As each bit of a word is written on the drum surface, the R PARITY flip-flop counts the number of binary 1s and produces a 13th bit to provide odd parity. When data is read from the drum, this flip-flop again counts the 1s and sets the parity error (PE) flip-flop, if an even number is detected in any one word. The condition of the PE flip-flop is indicated in the DCT as one of the two possible causes of an error condition. These circuits are shown in area C4 of engineering drawing BS-E-250-0-7 (BS-E-251-0-5).

2.3.10 Write Data and Writer

During a write cycle, data is presented on the read/write buses for recording on a selected drum track by the Drum NRZ Writer Type 4529 Module. The data is written as a function of the most significant bit of the DSB. This logic is shown in the lower right and left corners of engineering drawing BS-E-250-0-7 (BS-E-251-0-5).

2.3.11 Sector Counter (SC)

The SC is a 3-stage counter that recycles after an 8 count. The sector number (0 through 7) in the SC is compared with the DSA to permit writing (or reading) a word of the addressed sector on the drum. The SC contents increment after each word is shifted through the DSB (every 14th drum clock pulse). The contents of the SC are compared with the DSA to permit one word of a particular sector to be written.

2.3.12 Drum Memory

The drum memory block represents the rotating drum which stores the information received from the computer and the drum clock track timing.

2.4 DRUM WRITE CYCLE

(A quick reference source, table 2-1, Analysis of Instructions for the Write Cycle, is located at the end of this chapter.)

In general, the DRCW instruction (see table 5-1) initiates a drum write cycle in the drum control logic. The DRCW command normalizes certain control flip-flops in the drum control logic, sets the read/write flip-flop to the write state, sets the drum 4-state device to idle, sets the data

in/out signal to notify the computer data break facility that the transfer direction is out of the computer, loads the DCL from the accumulator, and sets the break request flip-flop to initiate a data break.

> NOTE: The drum control logic incorporates a 4-state device to signify drum control status. The four states are IDLE, TRA, ACT, and FLAG. Only one state is entered at a time, and during a normal transfer the states advance in sequence. Entry into any state disables all other states. The IDLE state indicates that the drum has not been activated by the program or it is waiting for a 200-μsec delay to set the TRA state. The TRA state indicates that the drum control is set up to transfer data, but the beginning of the drum track has not been encountered. The ACT state is entered at the beginning of the track to transfer data. The FLAG state indicates the completion of a sector transfer.

The break request signal, generated by the break request flip-flop, initiates a computer data break cycle. During the data break cycle, the DFB is loaded from the memory location specified by the DCL, and the contents of the DCL increment so that the next data break cycle addresses the next higher memory location. The drum control circuits now wait for the execution of the DRTS command (see table 5-1).

The DRTS command loads the drum track and sector address from the accumulator into the DTA and DSA registers. The DTA address register selects the specified track for the ensuing write cycle, and the DSA selects one sector of the track. The DFB register contents are transferred into the DSB register. The DRTS command also initiates a 200-μsec delay to permit the track selection circuits to set up.

After the 200-μsec delay, the TRA (transfer) state is set. The circuits now wait for the index pulse to signify the beginning of the track. The index pulse (first clock pulse after the 300-μsec gap on the drum) sets the 4-state device to ACT (active); if the sector counter is equal to the sector address (SC=DSA), writing begins immediately. If SC≠DSA, writing is inhibited until SC=DSA. Even though the SC may not be equal to the DSA, all operations of writing are performed, except that the NRZ writer is disabled.

For example, the ACT signal enables the drum clock pulses to generate the shift pulses and the write pulses (phase A pulses). The first word to be written is shifted into the DSB by the shift pulses. After a data bit is shifted into the most significant bit of the DSB (DSB0), the phase A pulse complements the write data flip-flop. If the NRZ writer is enabled, the data bit in DSB0 is written on the drum; if the NRZ writer is disabled, writing is simulated only. The control pulses continue shifting the contents of the DSB and writing the DSB0 contents (or simulate writing) until the twelve data bits and the parity bit are written. After the 13 bits are written, the DSB is again loaded from the DFB, and the circuits are set up to write another word. At this point the SC is incremented, and if SC=SA, the NRZ writer

is enabled, and the break request is sent to the computer to reload the DFB with the next word to be written. Writing continues in this manner until all 128 words of a sector are written. The end of track (beginning of the 300-μsec gap) sets the drum 4-state device to FLAG to indicate the completion of a sector transfer.

2.4.1 Detailed Discussion of Writing One Sector

The DRCW command (see table 5-1) executed by the computer starts the write cycle. The octal code of this IOT instruction is 6605. The execution of 6605 generates IOP1, IOP2, and IOP4 pulses in the computer. (Refer to the PDP-5 or -8 Users Handbook or the PDP-5 or -8 Maintenance Manual for the explanation of the IOT instruction.) Memory buffer bits 3 through 8 and the IOP pulses are applied to the Device Selector Type 4605, as shown in engineering drawing BS-D-250-0-5 (BS-D-251-0-4), coordinates C7. (Hereafter, drawing references shown only the last digit of the drawings and the coordinates. In the above case the reference is 5C7/4C7.) The internal gating structure of the 4605 circuit permits the IOT 6605 instruction to generate IOT 6601 and 6604 pulses (see table 2-1). Note that the IOT 6601 pulse sets the 4-state device to IDLE (5A5/4A5). The 4-state device can be in only one state at a time because the feedback from the current state disables the other three states.

After the DRCW execution, the DCL register contains the memory address of the first word to be written on the drum. The DRCW has set the break request flip-flop; therefore, the computer executes a data break cycle (table 2-1) to load the DFB from the memory location specified by the DCL register. The contents of the DCL register are incremented so that it addresses the next higher memory location. (Information on the computer data break cycle can be found in the PDP-5 or -8 Maintenance Manual.)

The control circuits now wait for the computer to execute the DRTS instruction. The DRTS instruction, 6615, applies MB bits 3 through 8 and the IOP pulses to the device selector (5C7/4C7) to generate the IOT 6611 and 6614 pulses. These pulses perform the operations outlined in table 2-1. In brief, they load the DTA and DSA registers from the accumulator, transfer the contents of the DFB into DSB, and trigger the 200-μsec delay which sets the TRA state (5B5/4B5).

The DSB is loaded with the word to be written, and assuming that the 200-μsec delay (5B5/4B5), which permits the track selection circuits to set up, is complete, the 4-state device is set to TRA. At this point the position of the drum is not known; therefore, the circuits must wait for the index pulse to signify the beginning of the drum track. Note that no phase A or phase B pulses are generated since ACT=0 (1C8X, 5C3/4C3). Therefore, the DSB is not shifted, and no writing occurs.

Note that if sector 0 is addressed, the DRTS instruction that loads the DSA also generates a data break cycle to transfer the second word to be written into the DFB. This is because the sector

counter is clear and SC=DSA. The TAKE WORD signal (generated during DRTS) is enabled by SC=DSA (5B2/4B2) to set the break request (RQ) flip-flop. Also, the DF ⟶ DSB signal (generated by DSB INI COND) enables the WRITE ENABLE flip-flop (7D7/5D7), since SC=DSA. The sector counter is clear at this time because a DONE signal clears the counter (4C1/3C1), and it remains clear through the previous nonactive cycles (ACT=0). Therefore, when sector 0 is addressed, at the beginning of the drum track, the DSB contains the first word to be written, the DFB contains the second word to be written, and the WRITE ENABLE flip-flop is enabled.

The index pulse generates the START pulse (5C2/4C2), which sets the 4-state device to the ACT state. The drum clock pulses are shaped by PG 1410 (5C2/4C2), whose output triggers the DONE/START 3.4-μsec integrating single shot. As long as there are clock pulses, the DONE/START multivibrator is held in the START state. In the absence of drum clock pulses, however, as during the 300-μsec gap, the DONE state is enforced. Hence, the index pulse sets the one-shot multivibrator to the START state, which in turn sets the 4-state device to ACT.

If the first four bits of the word to be written are 0011, as shown in the timing diagram in figure 2-7, the ACT signal (7D1/5D1) generates the 0B+ACT+DF ⟶ DSB pulse. This pulse enables the WRITE DATA circuits (7D2/5CS) to put the WRITE DATA flip-flop into the proper state to write the designated DSB0 bit at phase A pulse time. The ACT signal gating 0A (1C8X, 5C3/4C3) does not permit the index pulse to generate a phase A pulse. The second drum clock pulse generates the phase A pulse, and it complements the WRITE DATA flip-flop. The WRITE DATA flip-flop output is coupled to the NRZ Writer Type 4529 Module to write the designated bit. The ensuing phase B pulse generates the shift pulse (7B1/5B1), to shift the DSB. The phase B pulse, delayed to permit rise time of DSB0, generates the 0B+ACT+DF ⟶ DSB pulse which again establishes the proper state of the WRITE DATA flip-flop. The next phase A pulse writes the second bit specified by the DSB0 flip-flop.

After eleven shifts of the DSB register, DSB2 through DSB11 contain all 0s because the DSBS flip-flop, which is continually reset by the shift pulses, shifts 0s into the DSB. Note that the DF ⟶ DSB pulse initially sets DSBS; this insures 1 bits in DSB2 through DSB11 during the eleven shifts when a word is written, in the event that the DSB was originally clear. The twelfth shift pulse sets the OVERFLOW flip-flop (7C4/5C4), since DSB2 through DSB11 are all 0s. The OVERFLOW signal enables the R PARITY flip-flop to write the parity bit. The shift pulses complement the R PARITY flip-flop for each 1 bit that is written. Since the R PARITY flip-flop is initially set, an odd number of 1s leaves the R PARITY flip-flop in the reset state. In this case, the R PARITY^0 signal (1D10-M, 7D2/5D2) enables the 0B+ACT+DF ⟶ DSB pulse to reset the WRITE DATA flip-flop, so that the phase A pulse writes a 0 parity bit to generate odd parity.

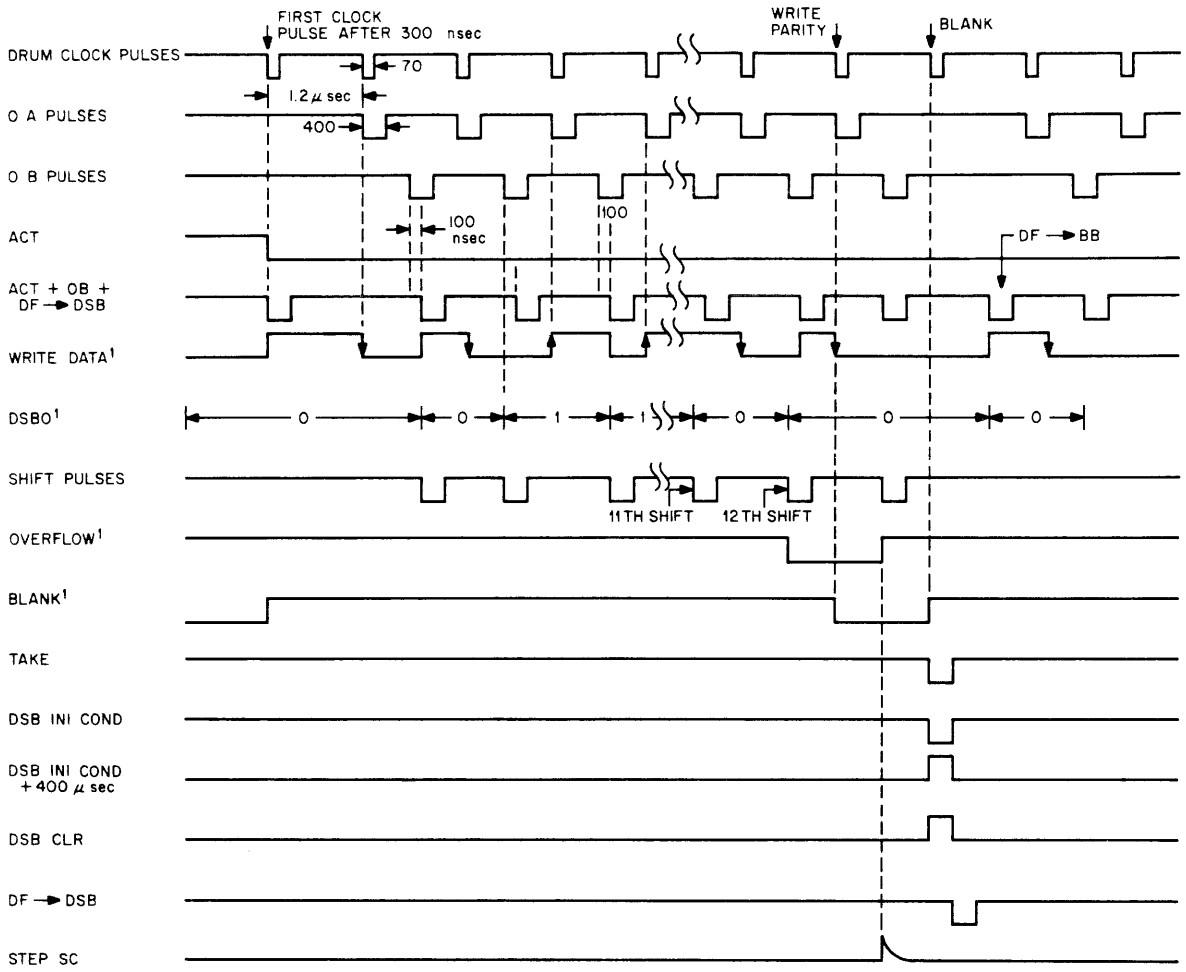


Figure 2-7 Write Cycle Timing Diagram

With the OVERFLOW flip-flop set, the next phase A pulse sets the BLANK flip-flop (5C4/4C4). The BLANK flip-flop inhibits the phase A and phase B pulses for one drum clock period (1C8Y, 5D2/4D2). Hence, a blank space (gap) separates the words written on the drum. The next phase B pulse resets the OVERFLOW flip-flop, and the next drum clock pulse resets the BLANK. When the last word on the track is written, the BLANK flip-flop remains set, since there are no more clock pulses to reset BLANK.

If the SC≠DSA, the actions described above still occur; but the WRITE ENABLE flip-flop is not enabled, and no writing actually occurs on the drum.

As the OVERFLOW flip-flop is reset by the 13th phase B pulse, the trailing edge of the OVERFLOW signal (4C4/3C4) increments the sector count. When the BLANK flip-flop is reset, the $BLANK^0$ signal (7C1/5C1) generates the TAKE WORD signal, which prepares the control circuits to

write the next 13-bit word. (Refer to table 2-1 for the sequence of events following the TAKE WORD signal.) Note that the DF ⟶ DSB pulse generates the 0B+ACT+DF ⟶ DSB pulse that prepares the WRITE DATA flip-flop to write the first bit of the next word. When the SC=DSA, the TAKE WORD signal (5B2/4B2) sets the RQ flip-flop to initiate a data break cycle to reload the DFB.

Writing continues until all 128 words of the addressed sector are written. The drum clock pulse that writes the parity bit of the 128th word of sector 7 (whether the NRZ writer is enabled or not) is the last drum clock pulse before the 300-μsec gap. The DONE/START one-shot multivibrator (5C2/4C2) reverts to the DONE state 3.4 μsec after the last drum clock pulse. The DONE signal (5B6/4B6) sets the 4-state device to the FLAG state. The ACT signal (4C4/3C4) increments the DSA count, so that the next sector (or track if SA=7_8) is addressed in case continuous sector transfers are specified by the program.

After the FLAG state is set, the actions that follow depend on the computer. If the computer is programmed to write only one sector, the DRSC instruction (octal code 6622) generates the IOT 6622 pulse to sense the FLAG state (1E10M, 5A7/4A7). When the FLAG state is 1, the I/O SKIP causes the computer to skip the next instruction and exit from the DRSC loop. The DRSE (code 6621) may then sense the drum control for errors. This is accomplished by the DRSE instruction, which generates the IOT 6621 pulse to sense the $PE^0 \cdot DE^0$ state (5A7/4A7). If no errors occur, the I/O SKIP signal causes the computer to skip the next instruction and exit from the drum write routine. If an error occurs, the program does not skip the next instruction which contains a JMP to an error check routine.

2.4.2 Writing Two Consecutive Sectors

When the computer is programmed to write more than one sector, instead of exiting from the write routine after one sector is written, the DRCN instruction causes writing to continue with the next sector. The DRCN instruction (refer to table 2-1) resets the PAR ERROR and DE flip-flops, generates TAKE WORD to prepare the control circuits to write the next word, and sets the 4-state device to TRA. With TRA set, the next index pulse sets the DONE/START multivibrator to START, which in turn sets the ACT state. The ACT enables the drum control circuits to write the next sector.

> NOTE: Because the drum track selection circuits require 200 μsec stabilization time, a new track must be specified during the first 100 μsec of the 300-μsec gap.

2.5 READ CYCLE

(A quick reference source table 2-2, Analysis of Instructions for the Read Cycle, is located at the end of this chapter.)

The DRCR instruction loads the DCL from the accumulator, normalizes control flip-flops in preparation for the read cycle, sets the 4-state device to IDLE, sets the DATA IN/OUT signal to

DATA IN, and sets the READ/WRITE flip-flop to read. The program executes the DRTS instruction to load the DTA and DSA registers from the accumulator and, after a 200-μsec delay, sets the TRA state. The next index pulse sets the ACT state, which enables the drum control circuits to read the drum. Data read from the addressed drum track is strobed into the least significant bit of the DSB register, and the contents of the DSB are shifted. After twelve shifts the DSB contains the word read from the drum; then parity is checked. If a parity error occurs, the parity error flip-flop is set to indicate the error. If the SC=DSA, the DSB contents are transferred to the DFB, and the break request signal is sent to the computer. The computer enters a data break cycle to transfer the DFB contents into the memory location specified by the DCL register. The DCL contents then increment. Transfer continues in this manner until all 128 words of the addressed sector are read. After the last word on the drum track is encountered, the FLAG state is set to signify the completion of the sector transfer.

2.5.1 Detailed Discussion of Reading One Sector

The DRCR instruction (octal code 6603) applies the MB bits 3 through 8 and the IOP pulses to the device selector, to generate the IOT 6601 and 6602 pulses. (Table 2-2 shows the detailed signal flow of the DRCR instruction.) In brief, the DRCR instruction sets the IDLE state, clears the READ/WRITE flip-flop, and loads the DCL from the accumulator. The READ/WRITE flip-flop remains clear to signify the READ state. The READ signal causes the DATA IN signal (5B7/4B7) to be −3v, to signify a DATA IN direction to the data break circuits in the computer.

The DRTS instruction is then executed to load the DTA and DSA registers with the drum track and sector address of the forthcoming read cycle. As shown in table 2-2, the DRTS instruction prepares the control circuits to read the first word. Note that a 1 is inserted into DSB11 (by DSB INI COND+400 nsec, 7C8) and the DSB register is cleared. After twelve shifts, the 1 inserted into DSB11 is in DSBF (7B2). Therefore, the $DSBF^1$ signal indicates that one word has been read from the drum. The read cycle timing diagram, figure 2-8, illustrates this condition.

After TRA is set, the control circuits wait for the index pulse. The index pulse sets the DONE/START one-shot multivibrator (5C2) to START, which in turn sets the 4-state device to ACT (5A6). The ACT signal (5C2) enables the drum clock pulses to produce phase A (0A), READ STROBE, and phase B (0B) pulses. As the drum rotates, the flux changes induce signals into the read heads. The addressed drum read head output is applied to the Type 1537 Sense Amplifier. The READ STROBE, occurring 0.25 μsec after the phase pulse, senses the sense amplifier (7C6) and produces a DATA READ pulse when a 1 is read from the drum; no pulse is produced when a 0 is read from the drum. The DATA READ pulse sets the DSBS flip-flop (7C8), and the shift pulse shifts the 1 from the DSBS into DSB11 as it shifts the DSB register.

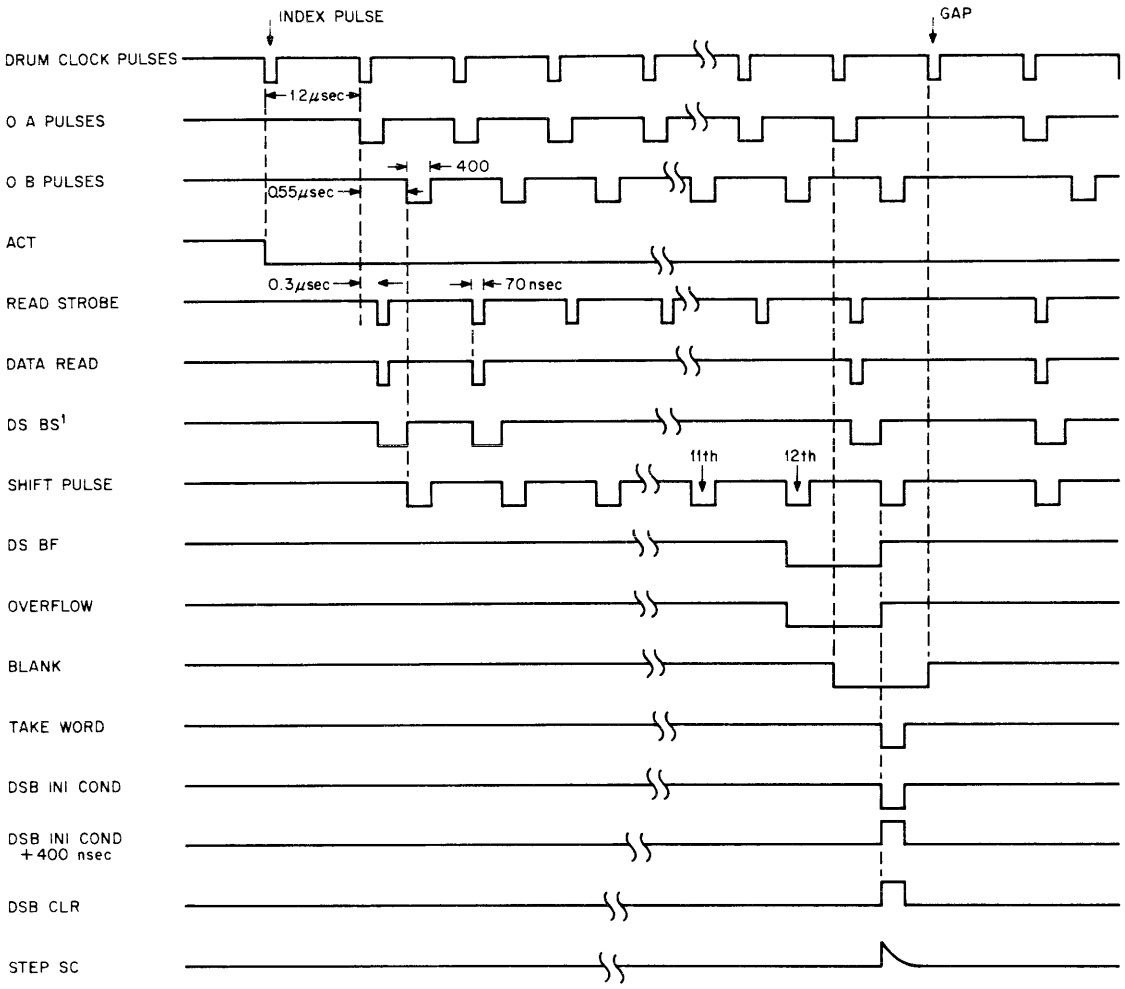


Figure 2-8 Read Cycle Timing Diagram

The shift pulse also resets the DSBS flip-flop. If the data bit read from the drum is 0, the DSBS flip-flop remains reset, and the shift pulse shifts a 0 into the DSB11 flip-flop. Data transfers continue in this manner until the original 1 bit that was in DSBS is shifted into DSBF. As the 1 is shifted into the DSBF flip-flop, the $DSBF^{1}$ signal sets the OVERFLOW flip-flop (7C4/5C4). The twelve bits read from the drum are in the DSB register. The next phase B pulse, enabled by READ and OVERFLOW, generates TAKE WORD and DSB INI COND (7C1/5B2). The DSB INI COND signal checks parity (explained later) and prepares the circuits to read the next word from the drum. If SC=DSA, the TAKE WORD (7B2/5B2), transfers the DSB contents into the DFB and sets the RQ flip-flop (5A2/4A2). The phase B pulse resets the OVERFLOW flip-flop, and $OVERFLOW^{0}$ (enabled by ACT, 4C3/4C3) advances the count of the sector counter.

When the RQ flip-flop is set, the word read from the drum is in the DFB. The RQ signal initiates a computer data break cycle to transfer the DFB contents into the memory location specified by the DCL (refer to table 2-2).

Data transfer continues in this manner until all words of the addressed sector are read. As the 300-μsec gap is encountered, clock pulses cease to occur and the DONE/START multivibrator reverts to the DONE state. The DONE signal sets the FLAG state. The trailing edge of the ACT signal (4C7/4C7) advances the count of the DTA and DSA registers. With the FLAG state set, the program senses the FLAG state to exit from the read routine.

2.5.2 Reading Two Consecutive Sectors

If the program designates consecutive sector transfers, the DRCN instruction (refer to table 2-2) is executed to read the next sector. The DRCN instruction must occur during the first 100 μsec of the 300-μsec gap.

2.5.3 Parity Check

As a word is read from the drum, the DATA READ pulse complements the R PARITY flip-flop (7C5/5C5). The R PARITY is initially set. The DATA READ pulse occurs only when a 1 is read from the drum. Since odd parity is generated during the write cycle, the R PARITY flip-flop must be in a reset state after the 12-bit word, plus the parity bit, is read from the drum. If not, the DSB INI COND pulse sets the PE flip-flop to indicate a parity error.

2.6 SPECIAL INSTRUCTIONS

2.6.1 DRCF Instruction

The DRCF (clear flag) instruction octal code 6611, generates the IOT 6611 pulse that resets the DE flip-flop (5B3/4B3), DTA (4C1/3B2-7), PE (7C4/5C4) and sets IDLE (5A4/4A4).

2.6.2 DREF Instruction

The DREF instruction loads the condition of the PE and DE into accumulator bits 0 and 1, respectively, to permit programmed evaluation of an error flag. The DREF instruction (octal code 6612) generates the IOT 6612 pulse. This pulse clears the AC (5C6/4C6) and generates a delayed 6612D pulse, which transfers DE to AC1 (5A4/4A4) and PE to AC0 (7D5/5D5).

2.7 DATA ERROR AND PARITY ERROR

The data error is generated when the computer does not answer a break request before another break request is made. The break request signal sets the ER SYNC flip-flop (5A3/4A3). The T5D pulse,

occurring during a data break, resets the ER SYNC. If a data break does not occur, the ER SYNC remains set. The next RQ signal is enabled by ER SYNC to set the DE (data error) flip-flop. (Parity error detection is explained above.)

2.7.1 Sensing PE·DE

The state of PE·DE is sensed by the DRSE (IOT 6621). The IOT 6621 senses the PE·DE signal and causes a program skip if no error occurs (5A8/4A8).

2.7.2 Maintenance Switch Control of PE·DE

In the ON position, the MAINTENANCE ON/OFF switch (5D2) applies $PE^0 \cdot DE^0$ to the gate (1D9F, 5C3/4C3), which enables the phase A, phase B, and READ STROBE pulses. Detection of a data error or a parity error inhibits the clock signals so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error. In the OFF position the equipment functions normally and data errors or parity error can be detected via the error flag at the end of a sector transfer.

2.8 DRUM TRACK SELECTION CIRCUITS

The drum track selection circuits are shown in engineering drawing BS-E-250-0-6 (BS-E-251-0-2). DTA bits 4 through 7 are applied to the Y selection circuits, and DTA bits 0 through 3 are applied to the X selection circuits. The addressed X selection circuit applies the read and write buses to a set of drum read/write heads. The addressed Y selection circuits provide a single return path for the group of read/write heads addressed by the X selection circuits. Hence, the DTA selects a single drum read/write head by the coincidence of the X and Y selection lines. For example, when the DTA is clear (DTA=000000000), the Y0 line and the X0 line select the read/write head that is labeled "0-7." The "0-7" refers to the eight sectors written by that read/write head. Similarly, all other read/write heads are labeled with their track and sector address.

2.8.1 FIELD LOCKOUT Switches

FIELD LOCKOUT switches are provided for retaining data on certain fields, so as to be available for reading only. There are eight FIELD LOCKOUT switches (figure 4-1). Each switch prevents writing on four drum tracks. Switch 1 inhibits tracks 0 through 3; switch 2 inhibits tracks 4 through 7; etc. Consequently, switch 8 inhibits tracks 34 through 37. The lockout is accomplished, as follows:

The DTA4 and DTA5 bits are applied to four decoders (4C5/3C5). Each decoder output LO_0 through LO_3 is a logic 1, when the bit contents of DTA4 and DTA5 are 00 through 11, respectively.

The WRITE signal is also an input to the decoders. The LO_0 through LO_3 signals are applied to the FIELD LOCKOUT switches as shown in 6D2 (2D2). When switch 1 is closed, LO_0 applies a negative potential to the X0 selection to prevent writing on the addressed track 0. Similarly, the other seven switches lock out their associated tracks.

2.9 POWER SUPPLY AND DISTRIBUTION (250 DRUM SYSTEM)

Primary power for the Type 250 Serial Drum is supplied by the computer. This power is supplied from the PDP-5 Power Control Type 832 as three lines: common, 115v via a contact of K1 and K3 (fast on-delayed off), and 115v via a contact of K2 (delayed on-fast off). Relays K1, K2, and K3 are in the Power Control Type 832. The fast-on delayed-off input supplies ac for the drum motor, blower motor, and the +10 and −15v power supplies in the Power Supply Type 779.

The common and delayed-on lines supply the primary power for the remaining half (red, yellow, and green terminals) of the Power Supply Type 779. (Refer to engineering drawing PW-C-250-0-19.) Normally both channels of this dual supply are operated from a single source of primary power. In the 250 System, however, the supply is modified so that each channel (each transformer) is operated individually. (Refer to engineering drawing RS-779.) The outputs from the orange, yellow, and blue terminals are connected to the red (+10), black (ground), and blue (−15) color coded connectors, respectively, on each mounting panel of modules. The +15 and −15v of the remaining channel (the common terminal remains unconnected) are connected in series. The result of this connection is −30v (−15 −15 = −30) provided for the NRZ Writer 4529, X Selection Modules 4530, Y Selection Modules 4531, and the isolation network shown at 7C6/7. This −30v potential is available after +10 and −15v power is applied to the modules.

A 12v dc relay is connected across the −15v terminal (refer to engineering drawing PW-C-250-0-19 and figure 2-9). The normally open contacts remove the −30vdc from the NRZ writer and X and Y selection circuits, and apply the 1-mc clock from the PDP-5 to 1C6F (5B4) to generate the DDC clear. After power is turned on the the −15v power supply rises to at least −12v, the relay energizes to remove the 1-mc clock and apply −30v to the NRZ writer and the X and Y selection circuits.

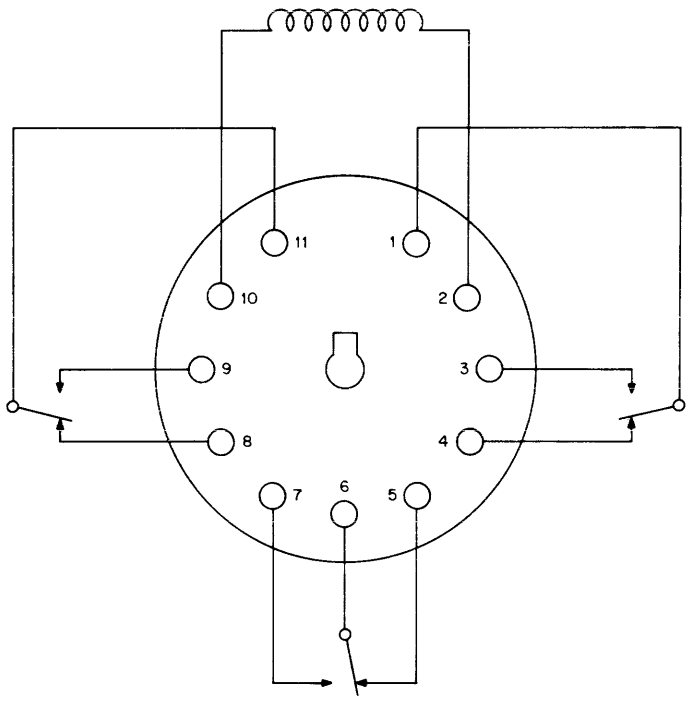


Figure 2-9 12v Relay Connections

2.10 POWER SUPPLY AND DISTRIBUTION (251 DRUM SYSTEM)

The 120 vac for the 251 Serial Drum is supplied by a 120-vac outlet. The ac is applied to the Power Control Type 832 in the 251 Drum System (refer to engineering drawing RS-832). Jumper wires connect terminals 1 to 3 and 4 to 5. Relay contacts in the 251 Drum 836 Power Control connect terminal 1 to 2, when the relay is energized; the relay is energized by −15v from the PDP-8 power supply (refer to engineering drawings PW-D-251-0-6 and RS-836). With the circuit breaker on and the REMOTE/LOCAL switch in the REMOTE position, ac power is supplied to relay contacts K1 and K2 when the −15v from the PDP-8 computer energizes the relay in the 836 Power Control. In the LOCAL position, ac power is applied to the K1 and K2 relays when the circuit breaker is on. The K2 contacts enable the fast-on delayed-off ac power. The K1 contacts apply ac to the time delay relay K3, which enables the delayed-on fast-off ac power.

The fast-on delayed-off ac power is applied to the blower fan, drum motor, and the +10 and −15v power supply in the Power Supply Type 779. The delayed-on fast-off ac power is applied to the dual 15v power supply in the Power Supply Type 779 (refer to engineering drawing RS-779). The red terminal of the 779 Power Supply is grounded, and the yellow terminal remains unconnected. This provides −30v at the green terminal, which is used in the NRZ writer, read sense amplifier, and in the X and Y selection modules.

When power is initially applied to the 251 Drum System, a DDC CLEAR pulse is generated to normalize control flip-flops in the drum control circuits. This is accomplished by the Type 4401 Module (refer to engineering drawing 251-0-4, coordinates D2) supplying DDC CLEAR pulses to the system. An RC network delays the −15v to terminal V of the 4401 Module. Shortly after the application of power, terminal V is sufficiently negative to inhibit the clock pulses and the drum can function normally.

2.11 DRUM MECHANICAL DESCRIPTION

2.11.1 Drum Head Mounting Description

The full complement of magnetic heads is mounted on the drum in a series of blocks, with a line of heads in each block, and the gaps coplanar at one surface, as shown in the simplified mechanical diagram, figure 2-10. The flat surface serves as the pad or slider of a hydrodynamic bearing, using the boundary layer of air clinging to the rotating drum as a lubricating or self-pressurizing medium. A single thin strip of spring steel connects each magnetic head/bearing pad to the drum frame. The spring steel reed serves as a combined motion pivot, loading spring, and mounting cantilever.

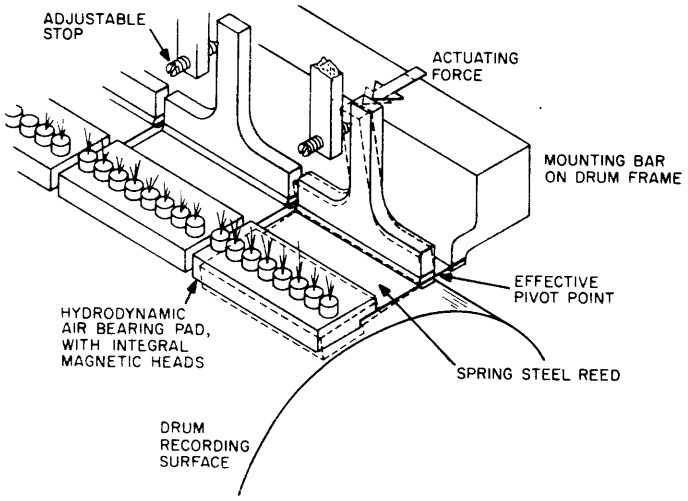


Figure 2-10 Drum Head Mounting

The action of this simple mechanical system for placing the magnetic head pad in close proximity to the drum surface, when the drum is at operating speed, is illustrated in figure 2-11.

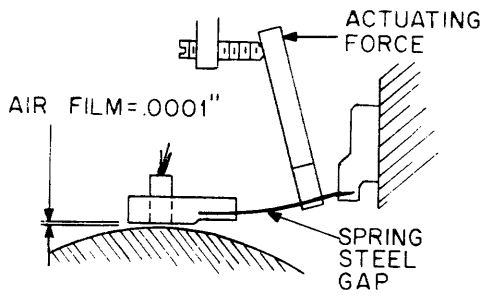


Figure 2-11 Operating Position of the Head Pad

2.11.2 Mechanical Actuator

The mechanical actuator moves the head into close proximity of the drum surface when the drum is up to speed. As the drum comes to speed, a centrifugal switch, mounted on the motor end, closes and sets a time-delay relay (red cap). The relay energizes in 1.5 min, and sets another time-delay relay (yellow cap), which supplies actuating power to the linear motor actuator for 6 sec. After the linear motor pulls in the heads, a holding coil, which is energized from rectified ac, holds in the heads. The 1.5-min delay permits the drum to reach full speed prior to actuation. The 6-sec interval must not be exceeded, because the linear motor has a very short duty cycle and can burn out if left energized. A circuit breaker, thermally actuated by the linear motor current, provides further protection for the motor.

Normal shut down of drum power or any power failure instantly raises the heads. Motor burnout, while not anticipated, results in speed loss, so that the centrifugal switch opens and raises the heads. A fuse mount, located under the right front corner of the cabinet, contains a switch for actuating the heads. The drum centrifugal switch must be closed to operate this switch. If holding coil fails to hold at the end of the pull-in cycle, the manual switch must be opened and closed to restart the cycle.

2.12 ANALYSIS OF INSTRUCTIONS

Table 2-1 and table 2-2 show the analysis of instructions for the write and read cycle, respectively. These tables provide a reference to detailed signal flow during a write or read cycle.

TABLE 2-1 ANALYSIS OF INSTRUCTIONS FOR WRITE CYCLE (continued)

Instruction, Operation, or Signal	Function
0A pulse	Complements WRITE DATA (7C5/5C5).
	Sets BLANK if OVERFLOW (5D4/4D4).
	Generates 0B pulse (5C5/4C5).
0B pulse	Resets OVERFLOW, if OVERFLOW = 1 (7C4/5C4).
	Generates SHIFT pulse if OVERFLOW = 0 (7B1/5B1).
	(Delayed) Generates 0B+ACT+DF → DSB pulse (7D2/5D2).
DRSC (6622)	Generates IOT 6622 pulse which senses the FLAG state (5A7/4A7).
DRCN (6624)	Generates IOT 6624 pulse.
IOT 6624 pulse	Clears PAR ERROR (7C4/5C4).
	Sets TRA state (5B5/3B5).
	Clears DE (5B3/4B3).
	Generates TAKE WORD (7C2/5C2).

TABLE 2-2 ANALYSIS OF INSTRUCTIONS FOR READ CYCLE

Instruction, Operation, or Signal	Function
DRCR (6603)	Generates IOT 6601 and 6602 pulses (5C7/4C7).
IOT 6601 pulse	(Via 1E11W, 5B1/4B1) Clears RQ, READ/WRITE, ER SYNC, DE, and via 1C11X (5A5) (1C11V(4A5)), sets IDLE.
	Generates DDC CLEAR (5B4/4B4), which clears OVERFLOW, R PARITY, PAR ERROR, WRITE DATA (7C4/5C4), and WRITE ENABLE (7D7/5D7).
IOT 6602 pulse	Clears DFB (7B2/5A2).
	Transfers AC to DCL (4B1/3B1).
	Clears AC (5C5/4C5).
DRTS (6615)	Generates IOT 6611 and 6614 pulses (5C7/4C7).

TABLE 2-2 ANALYSIS OF INSTRUCTIONS FOR READ CYCLE (continued)

Instruction, Operation, or Signal	Function
IOT 6611 pulse	Clears DTA and DSA; trailing edge transfers AC to DSA (4C4/3C6).
	Clears PAR ERROR (7C4/5C4).
	Clears DE (5B3/4B3).
IOT 6614 pulse	Transfers AC to DTA (4C1/3C1).
	Clears AC (5C5/4C6).
	Generates DSB INI COND (7C3/5C3).
DSB INI COND	Clears DSB and DSBF (7B2/5B2).
	Sets PAR ERROR if READ·ACT·R PARITY[1]=1 (7C5/5C5).
	Clears DSBS (7C8/5C8).
	Generates DSB INI COND+400 nsec which sets R PARITY and DSB11 (7C8/5C8).
0A pulse	Generates READ STROBE (5C4/4C4).
	Generates 0B pulse (5C4/4C5).
0B pulse	Generates SHIFT PULSE if OVERFLOW=0 (7B1/5B1).
	Resets if OVERFLOW=1 (7C4/5C4).
	Generates TAKE WORD when OVERFLOW=1 (7C1/5C1).
TAKE WORD	Generates DSB INI COND (7C2/5C3).
	Transfers DSB to DFB when SC=DSA (7B2/5B2).
	Sets RQ when SC=DSA (5B2/4B2).
DATA BREAK CYCLE	ADD to MA signal resets RQ and generates DRA (5B1/4B1).
	DRA increments DCL contents (4B8/3B8).
	T5 (T2) pulse from computer (5B2/4B2) resets ER SYNC and generates T5D (T2D); T5D (T2D) clears DFB (7A1/5A1).
DRSC (6622)	Generates IOT 6622 pulse which senses FLAG (5A7/4A7).
DRCN (6624)	Generates IOT 6624 pulse (5C8/4C8).
IOT 6624 pulse	Clears PAR ERROR (7C4/5C4).
	Sets TRA state (5B5/4B5).
	Clears DE (5B3/4B3).

CHAPTER 3
INTERFACE

All logic signals which pass between the computer and the serial drum are standard DEC levels or standard DEC pulses. A standard DEC level is either ground potential (0.0 to −0.3v) or nominal −3v. Standard DEC pulses are nominal 2.5v in amplitude (2.3 to 3.0v) and 0.4 μsec in duration (500 kc modules). Both positive and negative pulses are referenced to ground potential (0.0 to + 2.5v).

Throughout the manual, standard DEC ground-potential signals are symbolized by an open diamond (—◇) and standard DEC negative levels are indicated by a solid diamond (—◆). Open and solid arrow heads are used to symbolize standard DEC positive (—▷) and negative pulses (—▶).

In addition to the logic signal inputs, the computer power control unit provides ac power to the power supply and distribution network in the 250 Serial Drum. The ac power is used to energize or de-energize the serial drum from the computer during normal operation. In the 251 Serial Drum, an ac outlet supplies power to the 832 Power Control.

Input signals to the 250 Serial Drum are listed in table 3-1, and output signals are listed in table 3-2. The input and output signals for the 251 Serial Drum are listed in tables 3-3 and 3-4, respectively. Numbers in the serial drum drawing column of these tables indicate the engineering drawing number and the connector.

TABLE 3-1 INPUT INTERFACE FOR TYPE 250

Signal Name	Symbol	From PDP-5			To Type 250		
		Logic	Drawing	Connector	Logic	Drawing	Connector
AC_0^1	—◇	AC	BS-E-5-0-9	1J01-1	DCL	BS-D-250-0-4-B3	1F2-1
AC_1^1	—◇	AC	BS-E-5-0-9	1J01-2	DCL DTA	BS-D-250-0-4-B3 BS-D-250-0-4-C2	1F2-2

TABLE 3-1 INPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From PDP-5			To Type 250		
		Logic	Drawing	Connector	Logic	Drawing	Connector
AC_2^1	—◇	AC	BS-E-5-0-9	1J01-3	DCL DTA	BS-D-250-0-4-B4 BS-D-250-0-4-C2	1F2-3
AC_3^1	—◇	AC	BS-E-5-0-9	1J01-4	DCL DTA	BS-D-250-0-4-B4 BS-D-250-0-4-C3	1F2-4
AC_4^1	—◇	AC	BS-E-5-0-9	1J01-5	DCL DTA	BS-D-250-0-4-B5 BS-D-250-0-4-C3	1F2-5
AC_5^1	—◇	AC	BS-E-5-0-9	1J01-6	DCL DTA	BS-D-250-0-4-B5 BS-D-250-0-4-C4	1F2-6
AC_6^1	—◇	AC	BS-E-5-0-9	1J01-7	DCL DTA	BS-D-250-0-4-B6 BS-D-250-0-4-C4	1F2-7
AC_7^1	—◇	AC	BS-E-5-0-9	1J01-8	DCL DTA	BS-D-250-0-4-B6 BS-D-250-0-4-C5	1F2-8
AC_8^1	—◇	AC	BS-E-5-0-9	1J01-9	DCL DTA	BS-D-250-0-4-B7 BS-D-250-0-4-C5	1F2-9
AC_9^1	—◇	AC	BS-E-5-0-9	1J01-10	DCL SA	BS-D-250-0-4-B7 BS-D-250-0-4-C6	1F2-10
AC_{10}^1	—◇	AC	BS-E-5-0-9	1J01-11	DCL SA	BS-D-250-0-4-B8 BS-D-250-0-4-C6	1F2-11
AC_{11}^1	—◇	AC	BS-E-5-0-9	1J01-12	DCL SA	BS-D-250-0-4-B8 BS-D-250-0-4-C7	1F2-12
MB_3^0	—◆	MB	BS-E-5-0-9	1J01-27	DS	BS-D-250-0-5-C6	1F2-27
MB_3^1	—◆	MB	BS-E-5-0-9	1J01-28	DS	BS-D-250-0-5-C6	1F2-28
MB_4^0	—◆	MB	BS-E-5-0-9	1J01-29	DS	BS-D-250-0-5-C6	1F2-29
MB_4^1	—◆	MB	BS-E-5-0-9	1J01-30	DS	BS-D-250-0-5-C6	1F2-30

TABLE 3-1 INPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From PDP-5			To Type 250		
		Logic	Drawing	Connector	Logic	Drawing	Connector
MB_5^0	◆—	MB	BS-E-5-0-9	1J01-31	DS	BS-D-250-0-5-C6	1F2-31
MB_5^1	◆—	MB	BS-E-5-0-9	1J01-32	DS	BS-D-250-0-5-C6	1F2-32
MB_6^0	◆—	MB	BS-E-5-0-9	1J01-33	DS	BS-D-250-0-5-C6	1F2-33
MB_6^1	◆—	MB	BS-E-5-0-9	1J01-34	DS	BS-D-250-0-5-C6	1F2-34
MB_7^0	◆—	MB	BS-E-5-0-9	1J01-35	DS	BS-D-250-0-5-C6	1F2-35
MB_7^1	◆—	MB	BS-E-5-0-9	1J01-36	DS	BS-D-250-0-5-C6	1F2-36
MB_8^0	◆—	MB	BS-E-5-0-9	1J01-37	DS	BS-D-250-0-5-D6	1F2-37
MB_8^1	◆—	MB	BS-E-5-0-9	1J01-38	DS	BS-D-250-0-5-D6	1F2-38
IOP1	—▶	IOP Gen.	BS-D-5-0-6	1J01-40	DS	BS-D-250-0-5-C6	1F2-40
IOP2	—▶	IOP Gen.	BS-D-5-0-6	1J01-42	DS	BS-D-250-0-5-C6	1F2-42
IOP4	—▶	IOP Gen.	BS-D-5-0-6	1J01-44	DS	BS-D-250-0-5-C6	1F2-44
Power Clear	—▶	Power Clear Gen	BS-D-5-0-5	1J01-49 1J03-47	Drum Con-trol	BS-D-250-0-5-B4	1F2-49
MB_0^1	—◇	MB	BS-E-5-0-9	1J03-1	DFB	BS-E-250-0-7-B3	1F4-1

TABLE 3-1 INPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From PDP-5			To Type 250		
		Logic	Drawing	Connector	Logic	Drawing	Connector
MB^1_1	—◇	MB	BS-E-5-0-9	1J03-2	DFB	BS-E-250-0-7-B3	1F4-2
MB^1_2	—◇	MB	BS-E-5-0-9	1J03-3	DFB	BS-E-250-0-7-B4	1F3-3
MB^1_3	—◇	MB	BS-E-5-0-9	1J03-4	DFB	BS-E-250-0-7-B4	1F3-4
MB^1_4	—◇	MB	BS-E-5-0-9	1J03-5	DFB	BS-E-250-0-7-B5	1F3-5
MB^1_5	—◇	MB	BS-E-5-0-9	1J03-6	DFB	BS-E-250-0-7-B5	1F3-6
MB^1_6	—◇	MB	BS-E-5-0-9	1J03-7	DFB	BS-E-250-0-7-B6	1F3-7
MB^1_7	—◇	MB	BS-E-5-0-9	1J03-8	DFB	BS-E-250-0-7-B6	1F3-8
MB^1_8	—◇	MB	BS-E-5-0-9	1J03-9	DFB	BS-E-250-0-7-B7	1F3-9
MB^1_9	—◇	MB	BS-E-5-0-9	1J03-10	DFB	BS-E-250-0-7-B7	1F3-10
MB^1_{10}	—◇	MB	BS-E-5-0-9	1J03-11	DFB	BS-E-250-0-7-B7	1F3-11
MB^1_{11}	—◇	MB	BS-E-5-0-9	1J03-12	DFB	BS-E-250-0-7-B8	1F3-12
1 MC Clock	—▶	Timing Signal Gen	BS-D-5-0-17	1J01-45	Drum Control	PW-C-250-0-19	1F3-45

TABLE 3-1 INPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From PDP-5			To Type 250		
		Logic	Drawing	Connector	Logic	Drawing	Connector
SP0	⟶	SP Gen	BS-D-5-0-5	1J03-46	Drum Con-trol	BS-D-250-0-5-B1	1F3-46
Address ⟶ MA	⟶▷	MA Con-trol	BS-D-5-0-7	1J03-49	Drum Con-trol	BS-D-250-0-5-B1	1F3-49
T5	⟶	Tim-ing Signal Gen	BS-D-5-0-17	1J03-40	Drum Con-trol	BS-D-250-0-5-B2	1F4-40

TABLE 3-2 OUTPUT INTERFACE FOR TYPE 250

Signal Name	Symbol	From Type 250			To PDP-5		
		Logic	Drawing	Connector	Logic	Drawing	Connector
PE → AC_0	→	Drum Control	BS-E-250-0-7-D5	1F2-13	IM	BS-D-5-0-14	1J01-13
DE → AC_1	→	Drum Control	BS-D-250-0-5-A4	1F2-14	IM	BS-D-5-0-14	1J01-14
Skip	→	Drum Control	BS-D-250-0-5-A8	1F2-25	Skip Control	BS-D-5-0-8	1J01-25
Program Interrupt	◇	Drum Control	BS-D-250-0-5-A8	1F2-26	Prog Intpt Sync	BS-D-5-0-8	1J01-26
0 → AC	→	Drum Control	BS-D-250-0-5-C5	1F2-47	AC Control	BS-D-5-0-8	1J01-47
DFB_0^1	◇	DFB	BS-E-250-0-7-A3	1F4-13	MB	BS-E-5-0-9	1J03-13
DFB_1^1	◇	DFB	BS-E-250-0-7-A3	1F4-14	MB	BS-E-5-0-9	1J03-14
DFB_2^1	◇	DFB	BS-E-250-0-7-A4	1F4-15	MB	BS-E-5-0-9	1J03-15
DFB_3^1	◇	DFB	BS-E-250-0-7-A4	1F4-16	MB	BS-E-5-0-9	1J03-16
DFB_4^1	◇	DFB	BS-E-250-0-7-A5	1F4-17	MB	BS-E-5-0-9	1J03-17
DFB_5^1	◇	DFB	BS-E-250-0-7-A5	1F4-18	MB	BS-E-5-0-9	1J03-18
DFB_6^1	◇	DFB	BS-E-250-0-7-A5	1F4-19	MB	BS-E-5-0-9	1J03-19

TABLE 3-2 OUTPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From Type 250			To PDP-5		
		Logic	Drawing	Connector	Logic	Drawing	Connector
DFB_7^1	—◇	DFB	BS-D-250-0-7-D6	1F4-20	MB	BS-E-5-0-9	1J03-20
DFB_8^1	—◇	DFB	BS-E-250-0-7-A7	1F4-21	MB	BS-E-5-0-9	1J03-21
DFB_9^1	—◇	DFB	BS-E-250-0-7-A7	1F4-22	MB	BS-E-5-0-9	1J03-22
DFB_{10}^1	—◇	DFB	BS-E-250-0-7-A7	1F4-23	MB	BS-E-5-0-9	1J03-23
DFB_{11}^1	—◇	DFB	BS-E-250-0-7-A8	1F4-24	MB	BS-E-5-0-9	1J03-24
DCL_3^1	—◇	DCL	BS-D-250-0-4-A3	1F4-26	MA	BS-E-5-0-9	1J03-26
DCL_4^1	—◇	DCL	BS-D-250-0-4-A3	1F4-27	MA	BS-E-5-0-9	1J03-27
DCL_5^1	—◇	DCL	BS-D-250-0-4-A4	1F4-28	MA	BS-E-5-0-9	1J03-28
DCL_6^1	—◇	DCL	BS-D-250-0-4-A4	1F4-29	MA	BS-E-5-0-9	1J03-29
DCL_7^1	—◇	DCL	BS-D-250-0-4-A5	1F4-30	MA	BS-E-5-0-9	1J03-30
DCL_8^1	—◇	DCL	BS-D-250-0-4-A5	1F4-31	MA	BS-E-5-0-9	1J03-31
DCL_9^1	—◇	DCL	BS-D-250-0-4-A6	1F4-32	MA	BS-E-5-0-9	1J03-32
DCL_{10}^1	—◇	DCL	BS-D-250-0-4-A6	1F4-33	MA	BS-E-5-0-9	1J03-33
DCL_{11}^1	—◇	DCL	BS-D-250-0-4-A7	1F4-34	MA	BS-E-5-0-9	1J03-34

TABLE 3-2 OUTPUT INTERFACE FOR TYPE 250 (continued)

Signal Name	Symbol	From Type 250			To PDP-5		
		Logic	Drawing	Connector	Logic	Drawing	Connector
DCL^{1}_{12}	—◇	DCL	BS-D-250-0-4-A7	1F4-35	MA	BS-E-5-0-9	1J03-35
DCL^{1}_{13}	—◇	DCL	BS-D-250-0-4-A8	1F3-36	MA	BS-E-5-0-9	1J03-36
DCL^{1}_{14}	—◇	DCL	BS-D-250-0-4-A8	1F3-37	MA	BS-E-5-0-9	1J03-37
Break Request	—◇	Drum Con-trol	BS-D-250-0-5-A1	1F3-43	MSG	BS-D-5-0-6	1J03-43
Transfer Direction	*—◆	Drum Con-trol	BS-D-250-0-5-B7	1F3-44	MB Con-trol	BS-D-5-0-7	1J03-44

*Transfer direction is into computer from Type 250 when signal is at −3v level.

TABLE 3-3 INPUT INTERFACE FOR TYPE 251

Signal Name	Symbol	From PDP-8			To Type 251		
		Logic	Drawing	Connector	Logic	Drawing	Connector
AC_0^1	—◇	AC	BS-D-8-0-16	ME34D	DCL	BS-D-251-0-3-B3	1F1D
AC_1^1	—◇	AC	BS-D-8-0-16	ME34E	DCL DTA	BS-D-251-0-3-B3 BS-D-251-0-3-C2	1F1E
AC_2^1	—◇	AC	BS-D-8-0-16	ME34H	DCL DTA	BS-D-251-0-3-B4 BS-D-251-0-3-C2	1F1H
AC_3^1	—◇	AC	BS-D-8-0-16	ME34K	DCL DTA	BS-D-251-0-3-B4 BS-D-251-0-3-C3	1F1K
AC_4^1	—◇	AC	BS-D-8-0-16	ME34M	DCL DTA	BS-D-251-0-3-B5 BS-D-251-0-3-C3	1F1M
AC_5^1	—◇	AC	BS-D-8-0-16	ME34P	DCL DTA	BS-D-251-0-3-B5 BS-D-251-0-3-C4	1F1P
AC_6^1	—◇	AC	BS-D-8-0-16	ME34S	DCL DTA	BS-D-251-0-3-B6 BS-D-251-0-3-C4	1F1S
AC_7^1	—◇	AC	BS-D-8-0-16	ME34T	DCL DTA	BS-D-251-0-3-B6 BS-D-251-0-3-C5	1F1T
AC_8^1	—◇	AC	BS-D-8-0-16	ME34V	DCL DTA	BS-D-251-0-3-B7 BS-D-251-0-3-C5	1F1V
AC_9^1	—◇	AC	BS-D-8-0-16	MF34D	DCL SA	BS-D-251-0-3-B7 BS-D-251-0-3-C6	1F2P
AC_{10}^1	—◇	AC	BS-D-8-0-16	MF34E	DCL SA	BS-D-251-0-3-B8 BS-D-251-0-3-C6	1F2E
AC_{11}^1	—◇	AC	BS-D-8-0-16	MF34H	DCL SA	BS-D-251-0-3-B8 BS-D-251-0-3-C7	1F2H
MB_3^0	—◇	MB	BS-D-8-0-16	ME35M	DS	BS-D-251-0-4-C6	1F3M
MB_3^1	—◇	MB	BS-D-8-0-16	ME35K	DS	BS-D-251-0-4-C6	1F3K

TABLE 3-3 INPUT INTERFACE FOR TYPE 251 (continued)

Signal Name	Symbol	From PDP-8			To Type 251		
		Logic	Drawing	Connector	Logic	Drawing	Connector
MB_4^0	⟶◇	MB	BS-D-8-0-16	ME35S	DS	BS-D-251-0-4-C6	1F3S
MB_4^1	⟶◇	MB	BS-D-8-0-16	ME35P	DS	BS-D-251-0-4-C6	1F3P
MB_5^0	⟶◇	MB	BS-D-8-0-16	ME35V	DS	BS-D-251-0-4-C6	1F3V
MB_5^1	⟶◇	MB	BS-D-8-0-16	ME35T	DS	BS-D-251-0-4-C6	1F3T
MB_6^0	⟶◇	MB	BS-D-8-0-16	MF35E	DS	BS-D-251-0-4-C6	1F4E
MB_6^1	⟶◇	MB	BS-D-8-0-16	MF35D	DS	BS-D-251-0-4-C6	1F4D
MB_7^0	⟶◇	MB	BS-D-8-0-16	MF35K	DS	BS-D-251-0-4-C6	1F4K
MB_7^1	⟶◇	MB	BS-D-8-0-16	MF35H	DS	BS-D-251-0-4-C6	1F4H
MB_8^0	⟶◇	MB	BS-D-8-0-16	MF35P	DS	BS-D-251-0-4-D6	1F4P
MB_8^1	⟶◇	MB	BS-D-8-0-16	MF35M	DS	BS-D-251-0-4-D6	1F4M
IOP1	⟶	I/O Control	BS-D-8-0-16	MF34K	DS	BS-D-251-0-4-C6	1F2K
IOP2	⟶	I/O Control	BS-D-8-0-16	MF34M	DS	BS-D-251-0-4-C6	1F2M
IOP4	⟶	I/O Control	BS-D-8-0-16	MF34P	DS	BS-D-251-0-4-C6	1F2P

TABLE 3-3 INPUT INTERFACE FOR TYPE 251 (continued)

Signal Name	Symbol	From PDP-8			To Type 251		
		Logic	Drawing	Connector	Logic	Drawing	Connector
Power Clear	→	Timing	BS-D-8-0-16	MF34V	Drum Control	BS-D-251-0-4-B1	1F2S
MB^1_0	—◇	MB	BS-D-8-0-16	ME35D	DFB	BS-E-251-0-5-B3	1F3D
MB^1_1	—◇	MB	BS-D-8-0-16	ME35E	DFB	BS-E-251-0-5-B3	1F3E
MB^1_2	—◇	MB	BS-D-8-0-16	ME35H	DFB	BS-E-251-0-5-B4	1F3H
MB^1_3	—◇	MB	BS-D-8-0-16	ME35M	DFB	BS-E-251-0-5-B4	1F3M
MB^1_4	—◇	MB	BS-D-8-0-16	ME35S	DFB	BS-E-251-0-5-B5	1F3S
MB^1_5	—◇	MB	BS-D-8-0-16	ME35V	DFB	BS-E-251-0-5-B5	1F3V
MB^1_6	—◇	MB	BS-D-8-0-16	MF35E	DFB	BS-E-251-0-5-B6	1F4E
MB^1_7	—◇	MB	BS-D-8-0-16	MF35K	DFB	BS-E-251-0-5-B6	1F4K
MB^1_8	—◇	MB	BS-D-8-0-16	MF35P	DFB	BS-E-251-0-5-B7	1F4P
MB^1_9	—◇	MB	BS-D-8-0-16	MF35S	DFB	BS-E-251-0-5-B7	1F4S
MB^1_{10}	—◇	MB	BS-D-8-0-16	MF35T	DFB	BS-E-251-0-5-B7	1F4T
MB^1_{11}	—◇	MB	BS-D-8-0-16	MF35V	DFB	BS-E-251-0-5-B8	1F4V

TABLE 3-3 INPUT INTERFACE FOR TYPE 251 (continued)

Signal Name	Symbol	From PDP-8			To Type 251		
		Logic	Drawing	Connector	Logic	Drawing	Connector
Address → MA	⟶▷	MA Control	BS-D-8-0-10	PF35	Drum Control	BS-D-251-0-4-B1	1F8S
T2	⟶▷	Timing	BS-D-8-0-9	MF34T	Drum Control	BS-D-251-0-4-B2	1F2T

TABLE 3-4 OUTPUT INTERFACE FOR TYPE 251

Signal Name	Symbol	From Type 251			To PDP-8		
		Logic	Drawing	Connector	Logic	Drawing	Connector
PE → AC_0	→	Drum Control	BS-E-251-0-5-D5	1F5D	AC	BS-D-8-0-2	PE2D
DE → AC_1	→	Drum Control	BS-D-251-0-4-A4	1F5E	AC	BS-D-8-0-2	PE2E
Skip	→	Drum Control	BS-D-251-0-4-A8	1F6K	PC Control	BS-D-8-0-10	PF2K
Program Interrupt	◇	Drum Control	BS-D-251-0-4-A8	1F6M	I/O Control	BS-D-8-0-10	PF2M
0 → AC	→	Drum Control	BS-D-251-0-4-C5	1F6P	AC Control	BS-D-8-0-3	PF2P
DFB_0^1	◇	DFB	BS-E-251-0-5-A3	1F9D	MB	BS-D-8-0-5	PE4D
DFB_1^1	◇	DFB	BS-E-251-0-5-A3	1F9E	MB	BS-D-8-0-5	PE4E
DFB_2^1	◇	DFB	BS-E-251-0-5-A4	1F9H	MB	BS-D-8-0-5	PE4H
DFB_3^1	◇	DFB	BS-E-251-0-5-A4	1F9K	MB	BS-D-8-0-5	PE4K
DFB_4^1	◇	DFB	BS-E-251-0-5-A5	1F9M	MB	BS-D-8-0-5	PE4M
DFB_5^1	◇	DFB	BS-E-251-0-5-A5	1F9P	MB	BS-D-8-0-5	PE4P
DFB_6^1	◇	DFB	BS-E-251-0-5-A5	1F9S	MB	BS-D-8-0-5	PE4S

TABLE 3-4 OUTPUT INTERFACE FOR TYPE 251 (continued)

Signal Name	Symbol	From Type 251			To PDP-8		
		Logic	Drawing	Connector	Logic	Drawing	Connector
DFB_7^1	—◇	DFB	BS-E-251-0-5-A6	1F9T	MB	BS-D-8-0-5	PE4T
DFB_8^1	—◇	DFB	BS-E-251-0-5-A7	1F9V	MB	BS-D-8-0-5	PE4V
DFB_9^1	—◇	DFB	BS-E-251-0-5-A7	1F10D	MB	BS-D-8-0-5	PF4D
DFB_{10}^1	—◇	DFB	BS-E-251-0-5-A7	1F10E	MB	BS-D-8-0-5	PF4E
DFB_{11}^1	—◇	DFB	BS-E-251-0-5-A8	1F10H	MB	BS-D-8-0-5	PF4H
DCL_3^1	—◇	DCL	BS-D-251-0-3-A3	1F7D	MA	BS-D-8-0-4	PE3D
DCL_4^1	—◇	DCL	BS-D-251-0-3-A3	1F7E	MA	BS-D-8-0-4	PE3E
DCL_5^1	—◇	DCL	BS-D-251-0-3-A4	1F7H	MA	BS-D-8-0-4	PE3H
DCL_6^1	—◇	DCL	BS-D-251-0-3-A4	1F7K	MA	BS-D-8-0-4	PE3K
DCL_7^1	—◇	DCL	BS-D-251-0-3-A5	1F7M	MA	BS-D-8-0-4	PE3M
DCL_8^1	—◇	DCL	BS-D-251-0-3-A5	1F7P	MA	BS-D-8-0-4	PE3P
DCL_9^1	—◇	DCL	BS-D-251-0-3-A6	1F7S	MA	BS-D-8-0-4	PE3S
DCL_{10}^1	—◇	DCL	BS-D-251-0-3-A6	1F7T	MA	BS-D-8-0-4	PE3T
DCL_{11}^1	—◇	DCL	BS-D-251-0-3-A7	1F7V	MA	BS-D-8-0-4	PE3V

TABLE 3-4 OUTPUT INTERFACE FOR TYPE 251 (continued)

Signal Name	Symbol	From Type 251			To PDP-8		
		Logic	Drawing	Connector	Logic	Drawing	Connector
DCL^{1}_{12}	—◇	DCL	BS-D-251-0-3-A7	1F8D	MA	BS-D-8-0-4	PF3D
DCL^{1}_{13}	—◇	DCL	BS-D-251-0-3-A8	1F8E	MA	BS-D-8-0-4	PF3E
DCL^{1}_{14}	—◇	DCL	BS-D-251-0-3-A8	1F8H	MA	BS-D-8-0-4	PF3H
Break Request	—◇	Drum Con-trol	BS-D-251-0-4-A1	1F8K	MSG	BS-D-8-0-6	PF3K
Transfer Direction	* —◆	Drum Con-trol	BS-D-251-0-4-B7	1F8M	MB Con-trol	BS-D-8-0-5	PF3M

*Transfer direction is into computer from Type 251 when signal is at −3v level.

CHAPTER 4
INSTALLATION AND OPERATION

4.1 SITE REQUIREMENTS

The installation site must provide floor space at least 24 inches wide and 28 inches deep, to accommodate the serial drum. At least 9 inches must be provided in front of the cabinet and 15 inches at the back of the cabinet to allow opening the doors for maintenance.

The 250 Serial Drum source of 115v, 60 cps, single-phase power is supplied by the computer. Power for the 251 Serial Drum is supplied from a 115 vac outlet. The required ac power for both serial drums is 8.0-amp starting surge current and 5.0-amp running current.

Ambient temperature at the installation site can vary between 32 and 105°F (0 to 41°C) without deleterious effect upon equipment operation. For normal operation, an ambient temperature range from 70 to 85°F is recommended.

4.2 SIGNAL AND POWER CONNECTIONS

All signal connections to the Type 250 Serial Drum are made at connectors 1F2 and 1F4. To mate with these connectors, a cable containing an Amphenol connector of the 115-114P series is required. Maximum signal cable length ought not exceed 5 ft. The input and output signals are defined in tables 3-1 and 3-2, and their wiring connections are given in engineering drawings A-250-13 and A-250-15. Similarly, the connections to the 251 Serial Drum are made at 1F1 through 1F10, or 1H1 through 1H10. 1H16 is used for memory extension control.

4.3 CONTROLS AND INDICATORS

Manual control of the serial drum is exercised through switches on the switch panel (figure 4-1). The function of these switches is, as follows:

MAINT ON/OFF	Allows maintenance personnel to select the normal or stop-on-error mode of operation. In the OFF position, the equipment functions normally, and data errors or parity errors can be detected only by the error flag at the end of a sector transfer. In the ON position detection of data error or parity error by the machine inhibits generation of clock signals (0A, Read Strobe, and 0B), so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error.

LOCAL/REMOTE /OFF (251 only)	In the REMOTE position, the PDP-8 computer controls the application of power to the serial drum. In the LOCAL position, power is supplied to the serial drum. In both LOCAL and REMOTE positions, the circuit breaker must be on before power is applied to the serial drum. In the OFF position power is turned off from the serial drum.
ON/OFF (250 only)	Applies ac power to the serial drum. The ac power is supplied from the computer; therefore, power must be turned on at the computer before this switch is effective.
FIELD LOCKOUT	Each switch can control inhibiting of a group of 4 consecutive tracks (4096 words) during writing so that the information stored on those tracks cannot be accidentally destroyed.

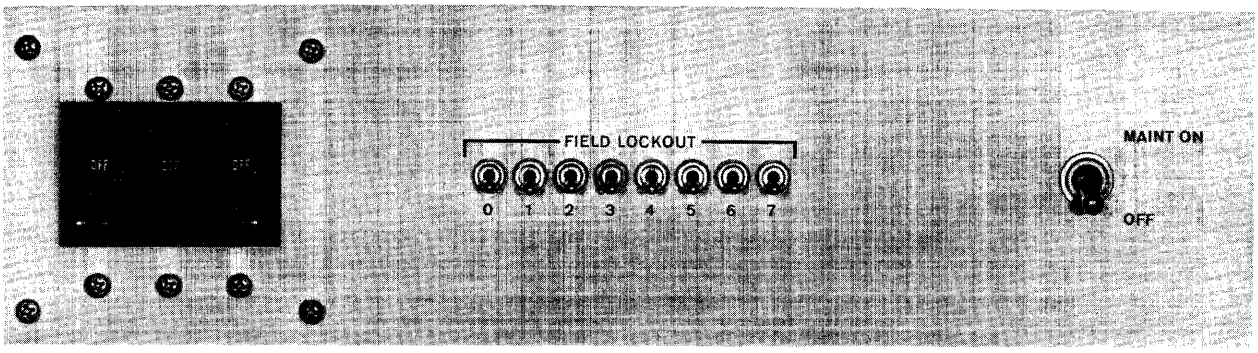


Figure 4-1 Switch Panel

Visual indication of the machine status and register contents is provided on the indicator panel (figure 4-2). The functions denoted by these lamps are as follows:

TRACK ADDRESS (11)	Light to indicate 1s in the drum track and sector address register.
CORE LOCATION (15)	Light to indicate 1s in the drum core location counter.

FINAL BUFFER (12)	Light to indicate 1s in the drum final buffer.
SERIAL BUFFER (12)	Light to indicate 1s in the drum serial buffer.
RD and WR	Light to indicate the machine is in either the read or write mode.
TRA	Light to acknowledge receipt of IOT pulse and indicate that the machine has been taken out of the IDLE state, and is waiting for clock pulses to be read from the drum to assure that the drum is in the correct position before initiating a transfer.
ACT	Lights to indicate that the machine has been taken out of the TRA (transfer) state and is actively engaged in a data transfer.
FLAG	Lights to indicate that a sector transfer has been completed and the machine has been taken out of the active state. The machine remains in this state until the flag is cleared when the machine is set to either the IDLE or the TRAnsfer state.
RQ	Lights to indicate that a data request signal has been sent to the computer to request a data break to transfer a word.
PE	Lights to indicate that the machine has detected a parity error after read-in from drum to core. If the MAINT ON/OFF switch is OFF when a parity error occurs, the drum error flag is set to 1; if the switch is ON, the IDLE state is set and the transfer terminated.
DE	Lights to indicate that the machine has detected a data error, because the data request signal from the drum was not answered before another request was given.

4.4 EQUIPMENT TURN-ON AND TURN-OFF

The operation of the 250 Serial Drum is controlled locally by the ON/OFF switch, provided power is available from the computer. When the ON/OFF switch is left in the ON position, the computer ON/OFF power switch controls application of power to the serial drum.

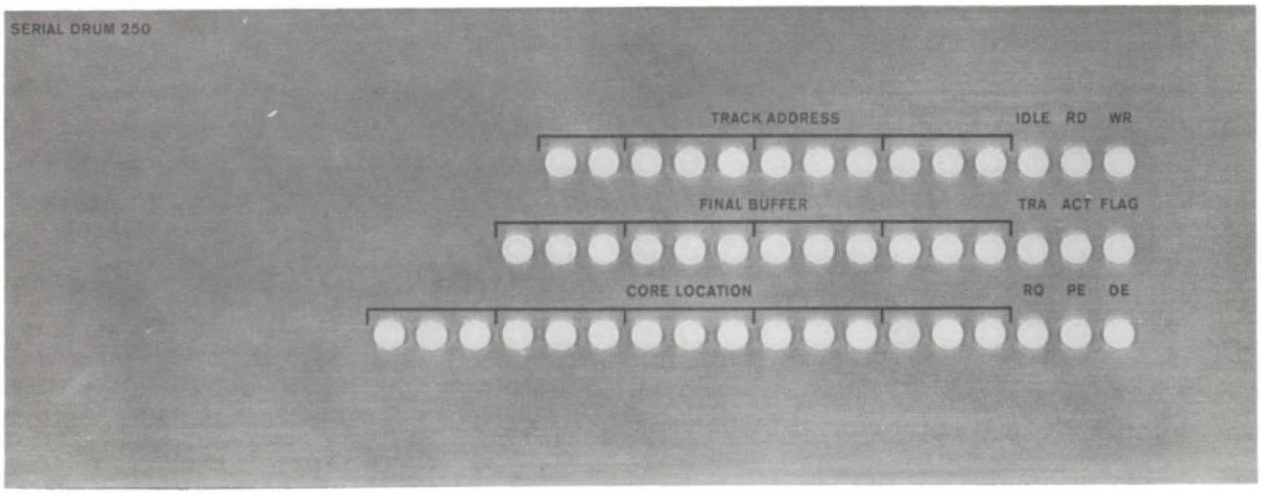


Figure 4-2 Indicator Panel

The operation of the 251 Serial Drum is controlled locally when the circuit breaker is on and the LOCAL/REMOTE/OFF switch is set to LOCAL; in the REMOTE position, the 251 Serial Drum is controlled by the PDP-8 computer.

CHAPTER 5
PROGRAMMING

5.1 IOT INSTRUCTION CODES

The operation of the 250 and 251 Serial Drums is controlled by the IOT instructions listed in table 5-1.

TABLE 5-1 TYPE 250 SERIAL DRUM INSTRUCTION LIST

Octal Code	Mnemonic Code	Operation
6603	DRCR	Load the drum core location counter with the core memory location information in the accumulator. Prepare to read one sector of information from the drum into the specified location.*
6605	DRCW	Load the drum core location counter with the core memory location information in the accumulator. Prepare to write one sector of information into the drum from the specified core location.*
6611	DRCF	Clear completion flag and error flag.
6612	DREF	Load the condition of the parity error and data timing error flip-flops of the drum control into bits 0 and 1 respectively, to allow programmed evaluation of an error flag.
6615	DRTS	Load the drum address register with the track and sector address held in the accumulator. Clear the completion and error flags, and begin a transfer (reading or writing).*
6621	DRSE	Skip next instruction if the error flag is a 0 (no error).
6622	DRSC	Skip next instruction if the completion flag is a 1 (sector transfer complete).
6624	DRCN	Clear error flag and completion flag, then initiate transfer of next sector.*

*The sector, track, and core memory addresses are suitably incremented and allow transfer of the next sequential sector with respecifying addresses. The DRCN instruction must be given within 200 μsec after the completion flag is set to 1 during the previous sector.

5.2 DRUM FORMAT AND PROGRAM TIMING

Chapter 2 explained the drum format, and showed diagrams of the drum format and word format. A sector transfer begins when the continuously rotating drum reaches the index mark, 1.2 μsec before the beginning of the data in a selected track and sector (word 0, bit 0). A 300-μsec interval separates the end of the last sector from the beginning of the first sector on each track.

Because the selection of the track read-write head requires 200 μsec stabilization time for continuous transferring, a new track must be specified during the first 200 μsec of the 300-μsec interval. If selected tracks and sectors are consecutive, uninterrupted transferring may be programmed merely by specifying continuation since the sector and/or track number and core memory location automatically increment. If a data timing or parity error occurs, however, the track and sector number are not advanced, and operations stop at the conclusion of the sector transfer. This feature allows the program to sense for error conditions and to locate the track and sector at which transmission fails. In general, the continuation command can be given any time within 200 μsec after the completion flag is set to 1.

The drum completion flag is set to 1 upon completion of a sector transfer, causing a program interrupt. The flag is cleared either by a clear flag (DRCF), or automatically when one of two transfer instructions (DRTS, DRCN) is given.

The error flag, which must be checked at the completion of each transfer, indicates either of the following two conditions:

a. A parity error is detected after reading from drum to core.

b. The data break request signal from the drum is not answered within the required 132-μsec period. This condition can occur, if other devices with higher priority are connected to the data break facility. Thus, in reading from the drum, the data word stored in core memory is incorrect; in writing on the drum, the next word has not been received from the computer.

5.3 PROGRAMMING SUBROUTINES

The following program examples indicate the operation of the drum system in single and multiple sector transfers.

5.3.1 Subroutine to Transfer (Read) One Sector

```
(1)             CLA             /CALLING SEQUENCE
(2)             TAD ADDR        /INITIAL CORE MEMORY ADDRESS
(3)             JMS READ
(4)             0
(5)             0
(6)     READ,   0
(7)             DRCR            /DRCW TO WRITE
(8)             TAD I READ      /LOAD AC WITH TRACK AND SECTOR ADDRESS
(9)             DRTS            /LOAD SERIAL DRUM DTA AND START TRANSFER
(10)            DRSC            /DONE?
(11)            JMP .-1         /NO
(12)            DRSE            /ERRORS?
(13)            JMP ERR         /JUMP TO ERROR CHECK ROUTINE
(14)            ISZ READ
(15)            JMP I READ      /RETURN
```

5.3.2 Subroutine to Transfer Successive (Two) Sectors

```
(1)             CLA             /CALLING SEQUENCE
(2)             TAD ADDR        /INITIAL CORE MEMORY ADDRESS
(3)             JMS READ
(4)             0               /TRACK AND SECTOR ADDRESS
(5)             0               /RETURN
(6)     READ,   0
(7)             DRCR            /DRCW TO WRITE
(8)             TAD I READ      /LOAD AC WITH TRACK AND SECTOR ADDRESS
(9)             DRTS            /LOAD SERIAL DRUM DTA AND DSA AND START
                                /TRANSFER
(10)            DRSC            /DONE?
(11)            JMP .-1         /NO
(12)            DRSE            /ERRORS?
(13)            JMP ERR         /JUMP TO ERROR CHECK ROUTINE
(14)            DRCN            /CLEAR FLAGS, CONTINUE TRANSFER OF
                                /NEXT SECTOR
(15)            DRSC
(16)            JMP .-1
(17)            DRSE
(18)            JMP ERR
(19)            ISZ READ
(20)            JMP I READ      /RETURN
```

The examples above use a programming technique common to subroutines which must be entered with several arguments. Memory addresses are not assigned in these locations; but the subroutines indicated above are numbered to simplify the following explanation. The first subroutine is repeated in the second example; therefore, the following discussion applies to both subroutines.

The first instruction (CLA) clears the accumulator, so that the core memory starting address of the data block to be transferred can be loaded into the accumulator by the second instruction (TAD ADDR). The third instruction is a jump to subroutine at address READ. In executing this instruction the contents of the program counter (which now contains the address of the fourth memory location) are stored in the sixth memory location (designated READ), the contents of the accumulator are unchanged, and program control advances to the seventh memory location. The DRCR instruction is executed to transfer the initial core memory address from the accumulator into the drum core location counter and to establish the read status in the drum. The next instruction is the TAD indirectly addressed from the READ location. At this time the READ location contains the 12-bit address of location four, deposited here as the contents of the program counter during the execution of the third instruction. Therefore, the TAD instruction loads the accumulator with the track and sector address.

The DRTS instruction transfers the track and sector information contained in the accumulator into the DTA and DSA registers, clears both drum flags, and initiates transfer. The DRSC instruction senses the drum completion flag and increments the contents of the program counter, if the flag is a 1,

thus indicating that the transfer is not complete; the program advances to the eleventh instruction which is a jump back to location ten to check the flag again. When the flag indicates that the transfer has been completed, the program advances to the twelfth instruction which is the DRSE instruction.

The DRSE instruction senses the error flag and skips the next instruction if no error has been detected. If an error has been detected, the error flag is 1 and the program advances to the next instruction to transfer program control to the error check routine. Finding no drum error, the program advances to the DRCN instruction. When the completion flag rises to indicate that a transfer is complete, the drum core location counter and the drum address register are already incremented, so that the execution of the DRCN instruction causes a transfer of the next successive sector. The DRCN instruction also clears the completion flag so that the transfer can take place. The next-to-last instruction is the ISZ at address READ. The READ location contains the address of the track and sector address (location 4). The ISZ instruction increments the contents of READ, so that it contains the address of the RETURN to the main program. Therefore, the JMP I READ instruction returns program control to the main program.

5.4 FIELD LOCKOUT SWITCHES

The FIELD LOCKOUT switches (figure 4-1) permit data to be retained on certain tracks where it is available for reading only. Turning a LOCKOUT SWITCH to the ON position inhibits writing on its associated track addresses. The octal addresses inhibited by each switch are shown below.

Switch	Addresses
1	000 to 037
2	040 to 077
3	100 to 137
4	140 to 177
5	200 to 237
6	240 to 277
7	300 to 337
8	340 to 377

CHAPTER 6
MAINTENANCE

Maintenance of the Type 250 and 251 Serial Drums consists of procedures repeated periodically, as preventive maintenance, and tasks performed after equipment malfunction, as corrective maintenance. Maintenance activities require use of the equipment (or equivalent) listed in table 6-1, and standard hand tools, cleansers, test cables, and probes.

TABLE 6-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Model
Multimeter	Triplett/Simpson	630-NA/260
Oscilloscope	Tektronix	540 Series
Variable Power Supply	DEC	734
System Module Extender*	DEC	1954
System Module Puller*	DEC	1960
Diagnostic Program	DEC	Digital-5-55-M

*Supplied with equipment

If it is necessary to remove modules, use the System Module Puller Type 1960. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the panel. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling.

To gain access to adjustment controls on the module, or to points for signal tracing, remove the module, and insert the System Module Extender Type 1954 into the proper module slot in the panel, and then reinsert the module into the extender.

6.1 PREVENTIVE MAINTENANCE

Perform preventive maintenance tasks prior to initial operation of the equipment, and periodically during its operating life. Perform these tasks in accordance with a reasonable schedule to check on progressive deterioration and to correct minor damage, thus, forestalling future failure. Compile a log book to record data found during the performance of preventive maintenance, to indicate the rate of circuit operating deterioration and provide information to determine when components should be replaced.

Preventive maintenance tasks consist of mechanical checks, such as cleaning and visual inspections, checks of specific circuit elements, such as the power supply, clock timing, sense amplifiers, and magnetic heads; and marginal checks to aggravate borderline conditions or intermittent failures, so that they can be detected and corrected. All preventive maintenance tasks must be performed every six months or 1,000 equipment operating hours, whichever occurs first.

6.1.1 Mechanical Checks

To assure good mechanical operation of the equipment, perform the following steps and the indicated corrective action for any substandard conditions found:

a. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-Kote (procured from Research Products Corporation, Madison, Wisconsin.)

c. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

d. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue enamel number 3277-1S65 or DEC gray enamel number 3277-1R44.

e. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security.

f. For mechanical security, inspect switches, knobs, jacks, connectors, transformers, fan, capacitors, and lamp assemblies.

g. Inspect modules for proper seating in the racks.

h. Inspect power supply capacitors for leaks, bulges, or discoloration.

6.1.2 Power Supply Checks

Check the output voltage and ripple content of the Power Supply Type 779. Check the +10v output between the yellow (-) and orange (+) connectors to assure that it is between 9.5 and 11.0v, with less than 800 mv ripple. Check the −15v and the +15v outputs (green to yellow and red to yellow, respectively) to assure that they are between 14.5 and 16.0v, with less than 400 mv ripple.

These supplies are not adjustable; thus, if the output voltage or ripple content is not within the tolerance specified, the supply is defective.

6.1.3 Timing Checks

Using the oscilloscope and referring to engineering drawing BS-D-250-0-5, check the timing of the Integrating Single Shot Type 4303 at location 1C4, and the Type 1304 Delay at location 1C15. If necessary, adjust the timing of these modules by turning the potentiomenter screw, which is accessible through a hole in the handle.

Check the single shot by observing the 1 output at 1C4W, while triggering the oscilloscope on 1C4K. During each revolution of the drum, the single shot is triggered every 1.2 μsec for approximately 17 msec during data reading, and receives no pulses during the 300-μsec gap. The output at terminal 1C4W must be at ground level during the gap, drop to −3v at the first triggering pulse, and remain at −3v for 3.4 μsec after the last triggering pulse is received before reverting to ground potential.

Check the timing of the delay module by observing the negative read strobe pulse at terminal 1C15E, while triggering the oscilloscope on the 0A pulse at 1C14J. Read strobe pulses must follow 0A pulses by approximately 0.25 μsec. Observe the read strobe pulses and the amplified output of a magnetic read head by connecting the second input of the dual-trace oscilloscope to terminal 1E25S. It is important that the read strobe pulses occur at the negative peak of the sinusoidal read signal. Measurements must be made using several different heads, and the read strobe pulse adjusted for an average of the measurements to eliminate large differences in peak playback time.

6.1.4 Drum Sense Amplifier Checks

The Type 1537 Drum Sense Amplifier modules at locations 1C1 (clock track) and 1E25 (data track) are checked for proper slice or threshold level at terminal S. This measurement can be made with the oscilloscope by measuring the amount the base line shifts above ground when the signal is connected to the input. The clock track sense amplifier slice level should be +100 mv. The data track sense amplifier slice level should be +150 mv. Adjustment of the slice level can be achieved by turning the potentiometer screw which is accessible through a hole in the module handle.

6.1.5 Drum Head Mounting Adjustments

Adjustment of the magnetic heads is provided by the stop screw for each pad of heads and its actuating arm, as shown in figure 6-1. With this stop screw properly positioned, the actuating arm moves the pad to a position where the reed is slightly bent and the pad is tangent to the drum surface at the line of head gap. These adjustments are made at the factory, and ordinarily need not be changed, at least no more than a minor adjustment. If adjustment is necessary, however, proceed as follows:

a. Connect an oscilloscope to 1E25S to observe the preamplifier output for the drum head in question.

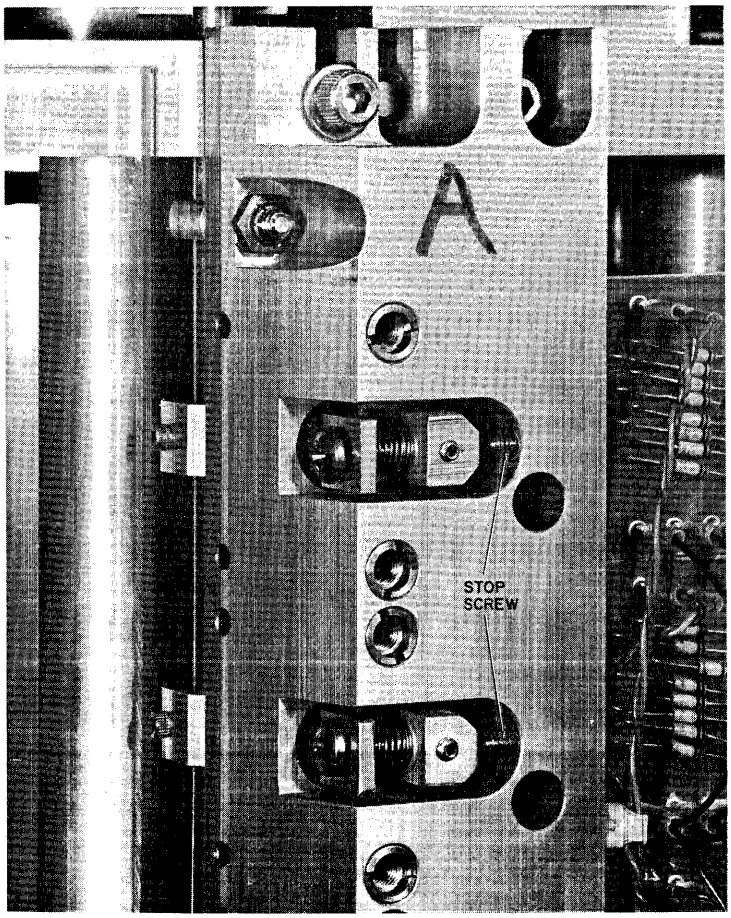
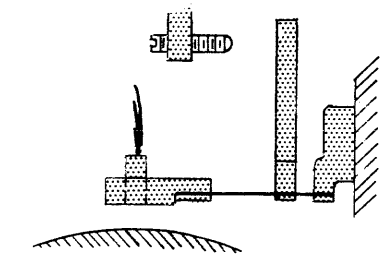


Figure 6-1 Stop Screw Position

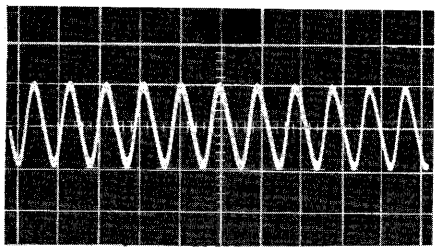
b. Set the DTA to address the drum head in question. Engineering drawing BS-E-250-0-6 (BS-E-251-0-5) shows the bar and pad location and the octal address of each drum head.

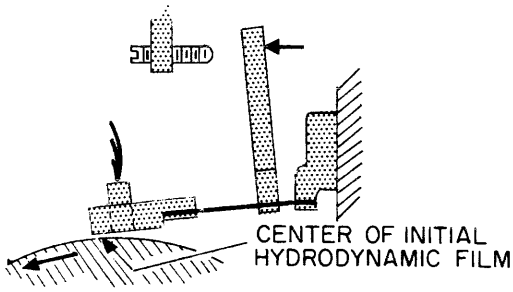
c. Set the drum control status to read.

d. Using a 5/64 hexagonal for socket heads, adjust the stop screws until a maximum output is noted on the oscilloscope as shown in figure 6-2. The adjustment screw is located on the right side of each bar as one views the drum, as shown in figure 6-1.

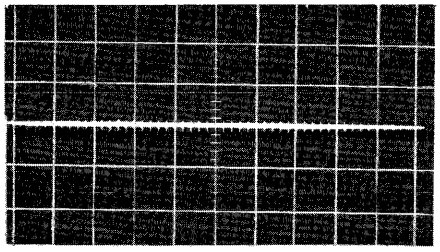


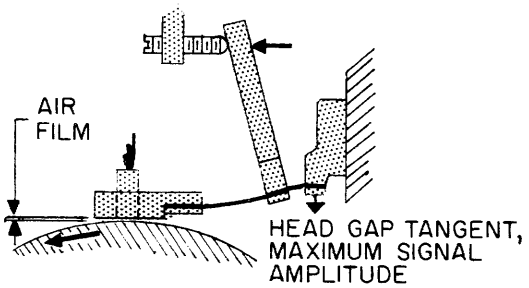
1. HEAD PAD RETRACTED



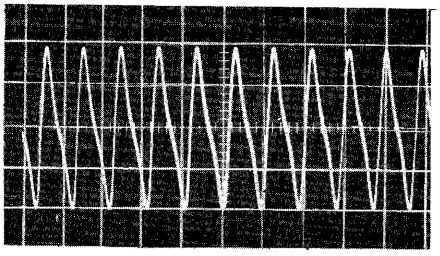


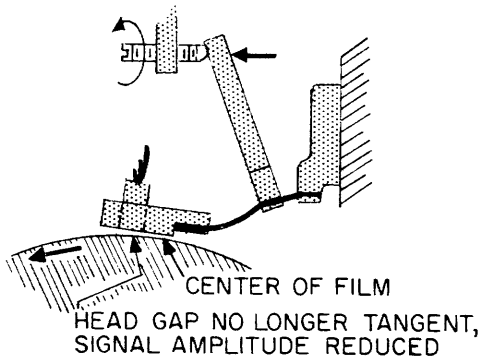
2. HEADS APPROACHING ROTATING DRUM





3. OPERATING POSITION





4. ADJUST STOP BACKED OFF TOO FAR

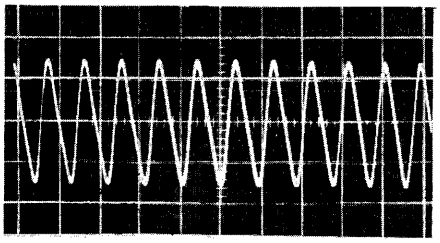


Figure 6-2 Operating Positions of Head Pad

CAUTION

If head adjustment is attempted with diode boards in place, make sure that the adjustment wrench is placed and/or insulated to prevent shorting connections or components to ground.

The best method of making this check is to run a program in which the patterns of all 0s, with all 1s, or alternate 1s and 0s on the selected track, and then read the data and monitor the output of the selected track. If data on the selected track is to be retained, it must be read into core memory before proceeding with this adjustment. Rewrite the selected track and read the recorded signal after every adjustment.

6.1.6 Pad Leveling Adjustment

The amplitude of head playback signals among the eight heads in each pad is set as uniformly as possible by using the pad leveling screws, which are accessible at the outer surface of each bar, roughly adjacent to the upper and lower edges of each pad. This may be checked on head number 1 (sector 0 → 7) and 8 (sectors 40 → 47) (top and bottom heads) with secondary reference to heads 2 and 7. Clockwise rotation of a pad leveling screw tends to increase signal amplitude at that end of the pad. Continuously write and read the selected heads, always alternating between the two.

6.1.7 Marginal Checks

Marginal checks are performed to aggravate borderline conditions within the logic to reveal observable faults, to permit correcting these conditions during scheduled preventive maintenance, to forestall possible future equipment failure. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. The checks are performed by operating the equipment logic circuits from an external, adjustable power source, such as the DEC Type 734 Variable Power Supply.

Raising the bias voltage above +10 is equivalent to lowering the amount of base drive on a particular transistor. This in turn simulates a lower gain driving transistor. Raising the bias voltage thus tends to indicate low gain transistors. Lowering the bias voltage below +10v simulates a condition where the voltage drop across the previous driving transistor (V_{CE}) increases; this tends to indicate high V_{CE} drop (leakage) transistors or low gain driving transistors. The −15v supply margins are not checked in the serial drum because raising or lowering the −15v does not affect the majority of control logic, since it is the collector load voltage and is usually clamped to −3v. The +10v margin should be about ±5v.*

*The 1537 Sense Amplifier, 1C1 and 1E25, has only ±2v margins on +10v.

Recording the level of bias voltage at which circuits fail permits plotting progressive deterioration and predicting expected failure dates, thereby setting up a method of planned replacement. Marginal checks of the +10 (A) supply (top switch at the left of the rack) to rack E vary the slice level on the drum sense amplifier modules, and therefore serve as a valuable tool in verifying the capability of the machine to read and write on the drum surface. Normally, increasing the +10 (A) supply by 3 or 4v also increases the slice level, and causes bits to be dropped out. Decreasing the +10 (A) source by 3 or 4v usually lowers the slice level, and causes bits to be picked up.

Marginal check terminals are provided on color-coded connectors connected in common to all racks, so that an external power supply can be connected to any connector to marginal check all racks. The color coding of these connectors from top to bottom is as follows:

Green, +10 vdc marginal-check supply

Red, +10 vdc internal supply

Black, ground

Blue, −15 vdc internal supply

Yellow, −15 vdc marginal-check supply

Three, single-pole, single-throw switches at the end of each rack of logic allow selection of either the normal internal power supply or the external marginal-check power supply for distribution to the logic. The top switch selects the +10v supply routed to terminal A of all modules in that rack. In the down position, the fixed internal +10v supply connected to the red terminal is supplied to the modules, and, in the up position, the marginal-check voltage supplied to the green terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10v level to terminal B of all modules. The bottom switch selects the −15v supply to be routed to terminal C of all modules. In the down position, the fixed −15v output of the internal power supply, received at the blue terminal, is supplied to the modules; in the up position, the marginal-check voltage, connected to the yellow terminal, is supplied to terminal C of all modules.

To perform marginal checks, proceed as follows:

a. Connect the external marginal-check power supply to the colored connector on any rack between the green (+) and the black (ground) terminal.

b. Energize the marginal-check power supply and adjust the outputs to supply the nominal +10 vdc.

c. Set the top switch on the rack to be checked to the up position.

d. Start equipment operation in a repetitive pattern or in a routine that fully utilizes the circuits in the rack to be tested. The diagnostic drum program, Digital-5-55-M, obtainable from the Digital Program Library, is recommended, unless a user has developed a special maintenance program.

e. Lower the +10v marginal-check power supply until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced.

f. Start equipment operation. Then decrease the +10v marginal-check supply until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced.

g. Stop operation and return the top switch to the down position.

h. Repeat steps b through g for the center switch on the logic rack being checked.

i. Repeat steps b through h for each rack or logic to be checked.

j. De-energize and/or disconnect the external marginal-check power supply.

6.2 CORRECTIVE MAINTENANCE

No special test equipment or tools are required for corrective maintenance, other than a broad bandwidth oscilloscope and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the system logic. Persons responsible for maintenance must become thoroughly familiar with the system concept and the operation of specific circuits as described in chapter 2, program techniques described in chapter 5, the engineering drawings presented in chapter 7, and the location of mechanical and electrical components.

Diagnosis and remedial action for a fault condition is performed in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the system.

b. System troubleshooting to locate the fault to within a module through the use of diagnostic programming, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of the malfunction.

e. Validation tests to assure that the fault has been corrected.

f. Log entry to record pertinent data.

6.2.1 System Troubleshooting

Do not attempt to troubleshoot the drum system without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks are required to assure that the serial drum is actually at fault before continuing corrective

maintenance procedures. Faults in equipment transmitting or receiving information or improper connections of the system frequently give indications very similar to those caused by drum malfunction. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault is determined to be within the serial drum, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the location of a fault is narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test is required to locate the source of the fault.

6.2.1.1 Diagnostic Program - Refer to program number DEC-5-55-M from the Digital Program Library.

6.2.1.2 Signal Tracing - If the fault is located within a functional logic element, program the equipment to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace a signal flow through the suspect logic element. Oscilloscope sweep may by synchronized by control signals or clock pulses available at individual module terminals. Trace the signal from the output back to its origin.

6.2.1.3 Aggravation Tests - Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive test cycle. Wiping the handle of a screwdriver across the back of a suspected row of modules is often a useful technique. By repeatedly starting the equipment and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

6.2.2 Circuit Troubleshooting

Where downtime must be kept at a minimum, a provisioning parts program may be adopted to maintain one spare module or standard component for insertion when system trouble-shooting procedures locate the fault to a particular component.

Bench troubleshooting procedures can be performed to correct the defective components. Where downtime is not as critical, the spare parts list can be reduced and signal tracing techniques utilized to troubleshoot modules within the equipment. This practice involves module removal by means of a Type 1960 System Module Puller, insertion of a Type 1954 System Module Extender into the logic rack, insertion of the suspect module in the module extender, and oscilloscope signal tracing of the module with the equipment energized and operating.

Static and dynamic circuit troubleshooting procedures may be performed at a bench. Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

a. Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

b. Do not attempt to measure resistance of any clock head. The voltage applied to the test probes is sufficient to erase information from the drum surface.

Measure the forward and reverse resistances of diodes. Diodes must measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistance of transistors. Most catastrophic failures are due to short circuits between the collector and the emitter, or an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally, 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction; open-circuit conditions exist in the reverse directions. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered as having both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection, and both the emitter and collector are assumed to be the cathode. Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Notethat although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. More reliable indication of diode or transistor malfunction is obtained through the use of one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by an intermittent connection, can be detected by connecting a 1.5v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cables and either a Type 722 or Type 756 Power Supply can be used to energize a system module. These supplies provide both the +10 vdc and −15 vdc operating supplies for the module, as well as ground, and −3v sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by logic level by means of eyelets provided on a Jones plug on the power cable. Type 911 Patch Cords may be used to make these connections on the Jones plug. In this manner logic operations and voltage measurements can be made. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

6.2.3 Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placement of excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers), which may be damaged by heat, the following special precautions must be observed:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6v-soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires, which are unsoldered or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals.

6.2.4 Head Pad Replacement

This replacement must be performed only by qualified personnel. To replace the head pads, the following tools are required:

a. Surface plate (at least 3 ft by 2 ft)

b. Two 2-inch machinists' parallels

c. Aligning pin, VRC (Vermont Research Corp.) part no. 59P7

d. Steel scale, 1/32-inch calibrations

e. Height comparator with 0.000,050 inch calibration (or finer), with less than 5-gram contact pressure. The "Electroprobe" manufactured by Federal Products, Providence, R.I., is suggested.

f. Adjustable height gauge, 3- to 4-inch micrometer caliper.

Replacement of the head pad must be done with the head mounting bar removed from the drum. This is done by removing the four socket head cap screws at the ends of the bar, disconnecting the matrix wiring, and setting the head mounting bar on the two parallels on the surface plate. Place the bar with the bearing surface of the pads upward, and the stop adjusting screws accessible at the edge of the surface plate.

Remove the head pad by removing screws at the pad and those holding the leads with a strain relief and the associated connector. Insert the new pad, bending the leads gently. Replace all screws. Check polarization of connector locating pins, which also serve as mounting screws, to ensure proper mating with the other half. Before tightening head pad mounting screws, insert the aligning pin through the corresponding hole in the bar and up into the aligning hole in the loose pad.

Insert aligning pin into the pad carefully making sure that no leads are caught at the pin hole. With the pin in place, scale the distance from each end of the pad to the reed mount and adjust the parallel within 1/64 inch. Tighten pad mounting screws and recheck parallelism. Remove the aligning pin and proceed to height adjustment.

Using housing flat-to-drum dimensions and the required drop allowance, measure the thickness of the bar and parallels in use, and calculate the height setting for the height gauge as follows:

HOUSING-TO-DRUM DIMENSION - DROP ALLOWANCE = REQUIRED BAR-TO-HEAD DIM.

REQUIRED BAR-TO-HEAD PAD DIM + PARALLEL THICKNESS + BAR THICHNESS = HEIGHT GAUGE SETTING

Set the height gauge to size, using the micrometer caliper; then use the height gauge to set the comparator to zero or center range. Rotate the actuator link and allow the head pad to move into actuated position. Using a hexagonal wrench in the corresponding stop screw, lower the pad being adjusted until the height comparator reads approximately zero at the center of the pad. Check elevation of the entire pad. Using the two differential pad leveling screws between the read mount and bar, and the stop screw for overall elevation, set the pad level within 0.0001 inch (leading to the trailing edge) and 0.0002 inch (end to end).

Replace the bar on the drum housing. Replace all matrix boards and wiring. Monitor the output signal from the replaced head pad (as described previously for head pad adjustment), while letting this pad approach the recording surface for the first time. As the stop screw is moved out,

allowing the actuator to move the pad into "flying position," compare output levels on heads 1 and 8 (top and bottom) in the pad. Balance these levels with ±10% with the differential screw adjustment at partial output levels; then move the stop screw out further until the "peaking" process (described under head adjustment) is complete.

6.2.5 Validation Test

Following the replacement of any electrical component of the equipment, a test is necessary to assure the correction of the fault condition and to make any adjustments of timing or signal levels caused by the replacement. This test is taken from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor is replaced in the proper supply, the ripple check for that power supply must repeat as specified under power supply checks. If repairs or replacemtns are made in any area not checked during preventive maintenance, the diagnostic program must be run or an appropriate operation test devised. For example, if a flip-flop is repaired or replaced, checking the register or control function performed by the flip-flop in entirety by manually setting and clearing, by programmed exercise of the function, or by repeating the diagnostic program, is required.

6.2.6 Log Entry

Corrective maintenance activities are not completed until recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments helpful for maintaining the equipment in the future.